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ARTICLE

Proficient Technique for High Performance Very Large-Scale Integration System to Amend Clock Gated Dual Edge Triggered Sense Amplifier Flip-Flop with Less Dissipation of Power Leakage

A. N. Duraivel[1,*], B. Paulchamy[2], and K. Mahendrakan[2]

Clocked flip flops are used to memory in synchronous or clocked series networks, adjusting the individual clock signal status. Therefore, at these times of clock signal transfer, the state of the memory unit and the state of the whole electrical structure change. It's only during signal transfer that the key to a flip-flop being correctly operated. Two transitions from 0 and 1 are followed by a clock pulse, and 1 to 0. The pulse shift is defined by the positive and negative sides of the pulse. The data on or off the clock cycle edges are recorded by a single-edge trigger flip flop (SETFF), but the flip flop with the double-edge sensor amplifier (DETSAFF). Another common technique for dynamic energy consumption reduced when the device is idle is the clock gating. In this document. Sleep is used to reduce the power of the leakage Here are the following: High threshold voltages sleep transistors are used. Among the supply voltage and VDD the sleep pMOS transistor and the pull-up system and between the network and the ground GND a sleep NMOs Transistor is located. With sleep transistors, CG-SAFF can save up to 30% of its power during zero input switching operation. For different sequential device architecture, the proposed flip-flop may be used.

Keywords: Pull-Up Network and Pull-Down Network, Sense Amplifier (SA), Sleep Method, Zero Input Switching Activity, Clock Gated Sense Amplifier Flip-Flop (CGSAFF), Dual Edge Triggered Sense Amplifier Flip-Flop.

1. INTRODUCTION

In Field of Very Large-Scale Integration System (VLSI), the power consumption factor is controlled by the clock system sources. The proposed clock system involves the clock distribution network and Flip-Flops (FF). FLIP-FLOPS (FF) has a higher rate and less power consumption and is one of complex systems with complicated clocking elements. Its performance analysis is the main factor for an analysis of the entire synchronization circuit's performance. Normally, SETFF uses one clock edge, another clock edge is idle, but on both sides of the clock cycle rising and dropping edge, DETFF fetches input data. Since both clock edges are involved in the flip-flop activated dual edge (DETFF), the data output is doubled when the SETFF works at half of its clock frequency. Many low-energy DETFF systems have now been suggested. A flip flop (FF), which is the Dual Edge Sense Amplifier flip flop (DETFF) power efficient system, is divided into two major classes: pulse DETFF, master-slave DETFF activated. The DETFF's master-slave are built by negative as well as positive clock edge flip-flops in parallel. DETFF caused by pulses has individual one phase and is of compact logic circuit complexity. The input clock gating strategy is practical to decrease complex power usage to minimize redundant changes in the pulse generator of DETSAFF [1]. The use of sleep technology in the synchronous method to minimize more dissipation of the power of the leaks related to idle block design.

The following portion is part of this planned work. The current Section 2 has the current memory unit and Clock gated Dual Edge Sensual Amplifier Flip-Flop amplifier that is activated by the double edge. Then Section 3 Explain the new approach to reducing the

[1]Electronics and Communication Engineering, Kings Engineering College, Chennai 602117, Tamilnadu, India
[2]Electronics and Communication Engineering, Hindusthan Institute of Technology, Coimbatore 641032, Tamilnadu, India
*Author to whom correspondence should be addressed.
Email: duraivel.n@gmail.com
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dissipation of leakage further. Up to 30% of the energy savings discussed in Part IV of the Sleep Transistor CGSAFF will achieve. In Section 5, the work is finally outlined.

2. LITERATURE SURVEY

The timing components of the integrated circuit (flip-flops and latches) (IC). Flip flops are often used as a timing feature in the IC as storage elements that use more power. One of the common methods of reducing power consumption is the dual-edge triggering principle. Since both the flip-flop (DETFF), which is triggered by the dual-edge, does not fade, therefore, the data flow is high relative to the flip-flop triggered by a traditional one-edge. The (1) Latch-Mux category and (2) flip-flop pulse are two key divisions [1] of the DETFF. Two levels, a master and a slave consist of the latch-mux. These two stages are organised in parallel, one of which is translucent at one level of the clock, and another one at the opposite level of the clock is again transparent. The second form, pulse, caused flip-flops into two more subcategories: (1) Implicit and (2) Explicit. The pulse generator that produces pulses is used in both forms.

The pulse creator produces pulse inside the memory unit, which income the form of pulse is triggered tacit (IP-FF), while the pulse is produced outside the device (EP-FF). On the other hand if EP-FF control is additional than IP-FF, EP-FF is commonly consumed for clock distribution that delivers the pulse generator's overhead power. The definition of double-edge trigger is harder to incorporate into IP-FF, whereas EP-FF is suitable for dual-edge triggering. Various DETFFs were planned in designs for low power integrated circuit (ASIC) applications to reduce power consumption.

2.1. Discharging Controlled Flip-Flop Unit

The illustration figure is given in Figure 1 for static flip-flop discharge-controlled discharge (SCDFF). SCDFF has a double pulse generator [2, 4] and static latch arrangement in its overall structure. The clock pulse is externally produced here. This twist is known as an overt pulsed twist (EP-FF). Two static phases of the static latch structure. Transistors m2 (first stage) and m6 are injected into the external pulse (second stage).

The transistor m2 and m6 are activated during the sampling time. In the first step the transistor m to 1 and m3 is introduced into input D. If $D = 1$ and $Q = 0$ (assumption), the transistors m2, m3 and m4 discharge node X. As a outcome, in the second stage the output Q will immediately switch to high levels with a pull-up transistor m5. As long as D is high, node X is still short. The junction transistor m1 and m3 are supplemented by the D input (in the first step), m3 is turned off.

The feedback path is finally opened and the node X at some voltage is pre-charged. In the second step, the D inverted input is now used to discharge the m7 transistor, so that output Q is discharged through the m6 and m7 tracks. An additional transistor, m4, powered by a complementary programmed signal is controlled at node X for the unwanted discharge. The SCDFF is used primarily to minimize unnecessary switching operation with low power VLSI architecture.

2.2. Static-Pulsed Flip-Flop with Dual Edge Triggering Unit

Figure 2 displays a pulsed flip flop structural figure with a static triggering two-edge [4, 8] (DETSPF). The DETSPFF is made up of two components: (1) Circuit (2) Static latch explicit pulse generation. There are four inverters and two NMOS-pass transistors in the explicit pulse generator. The delayed and inverted signal, respectively CLK2 and CLK3, is produced. In the drain of the NMOS transistor N5, the delayed CLK2 clock signal is inserted at the similar period that the N5 gate can be operated by the CLK clock signal. The CLK3 inverted clock has been used in the channel of the other NMOS junction transistor N6, at which point the CLK1 inverted clock signal can be regulated at the time. These two signals produce a small sample window, as seen in the diagram, both on the elevated and dropping clock edges [16].

The N1 and N2 pass transistors are enabled to test data inputs during the sampling process. The D and DB data inputs are incorporated in the N1 and N2 transistors into the SB and S static nodes. It helps to keep the wait minimum. The floating of the SB and S static nodes are operated by the N3 and N4 weak NMOS transistors. If the data entry D is strong, the weak NMOS transistor N4 immediately loads the statistic node SB. The reversed data input will be tiny, while the NMOS transistor P2 upto Vdd will charge the static node S. During another sample time, D is low and the static node SB is modified to V through the PMOS transistor. Simultaneously with the feeble NMOS transistor N4 is unloaded the static node SB. The key purpose of DETSPFF is to remove unintended transformations. While the next input is the same as the previous input, the transformation inside the circuit happens again. This means an undesirable transition.

2.3. Adaptive Clocking Dual Edge Triggered Sense Amplifier Flip-Flop

The flip-flop sensor amplifier (ACSAFF) schematic diagram for adaptive clocking of dual edge [5, 14] is shown in Figure 3. ACSAFF is mostly assisted by Ref. [1] the inverter chain clock [2]. Circuit front end [3]. Latch. Latch. Latch. Used to create delayed clock signals is the clock inverter chain. The NC node is extracted from the front end circuit which, in low operation, disables the clock inverter chain [4]. Both CLK and CLK3 have been high on the CLK climbing edge for a small period and both

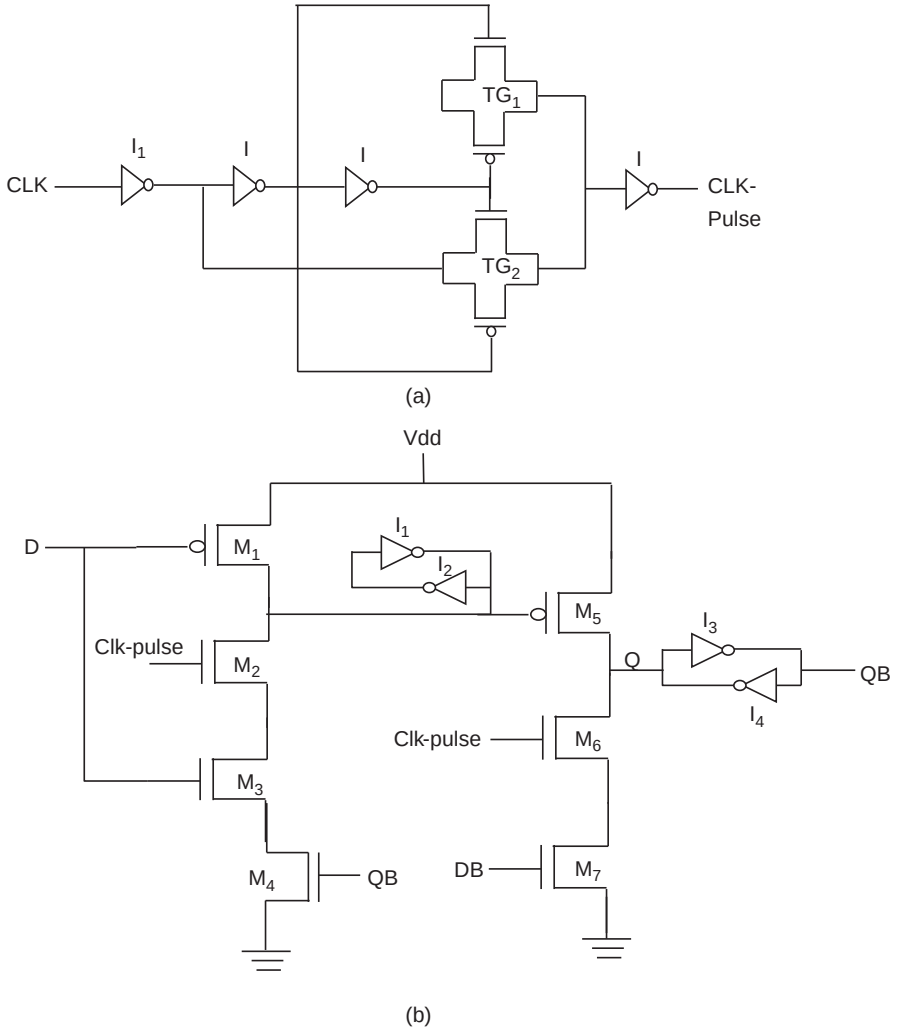

Fig. 1. Illustration diagram of proposed circuit (a) dual pulse generator (b) static latch.

CLK1 and CLK4 have both been very high on one CLK climbing edge for a small period. The delays on the front end circuit are applied. If D is not the same as Q data entry, the NC node is charged through N5 and N6 (or) N7 and N8 transistors. Inverted and delayed signals CLK3 and CLK4, the NIC1- and NIC2-transistor signals will be turned on to create the small sample window at the rising or dropping clock edges. The SB (or) RB Node creates an ACSAFF [5], I latch, unloading path during the narrow sample time. The NC node is pushed down via the N2 and the N1 (or) N3 and N4 transistors as the performance shifts when the NC node deactivates the inverter clock chain. If input D is equal to output, Q, SB and RB nodes will keep their previous output high and latch will keep it high. At low switching operation, ACSEFF saves more energy, but needs more junction transistor to incorporate input clocking.

2.4. Dual-Edge Triggered Sense Amplifier Flip-Flop

Figure 4 shows the diagram [4, 7] of the dual-edge flip-flop sensor amplifier (DET SAFF). The DETSAFF has three main components: (1) dual pulse generator to produce pulse signal on the edges of the up and down clock (2) sensing system dependent on the flip-flop sensory amplifier (SAFF) (3) Look. (3) Look. The DET SAFF is an overt form because the pulse signal is produced outside the system and added to a number of flip-flops. In the sensing system the PMOS transistor SP bin1 is enabled, while the node SB is preloaded to Vdd if input D is small (high). Similarly, the PMOS SP2 transistor is enabled when input D is high and the RB node is uploaded to Vdd (high). In this context, the PMOS transformation driven by input in the preload direction is SP1 and SP2.

When D is extreme, node SB is downloaded to DB at low rate via SN1 and node RB is preloaded to Vdd during the translucent time. Similarly, if D is low node, SB is pre-loaded with SP1uptoVdd and RB is discharged to low

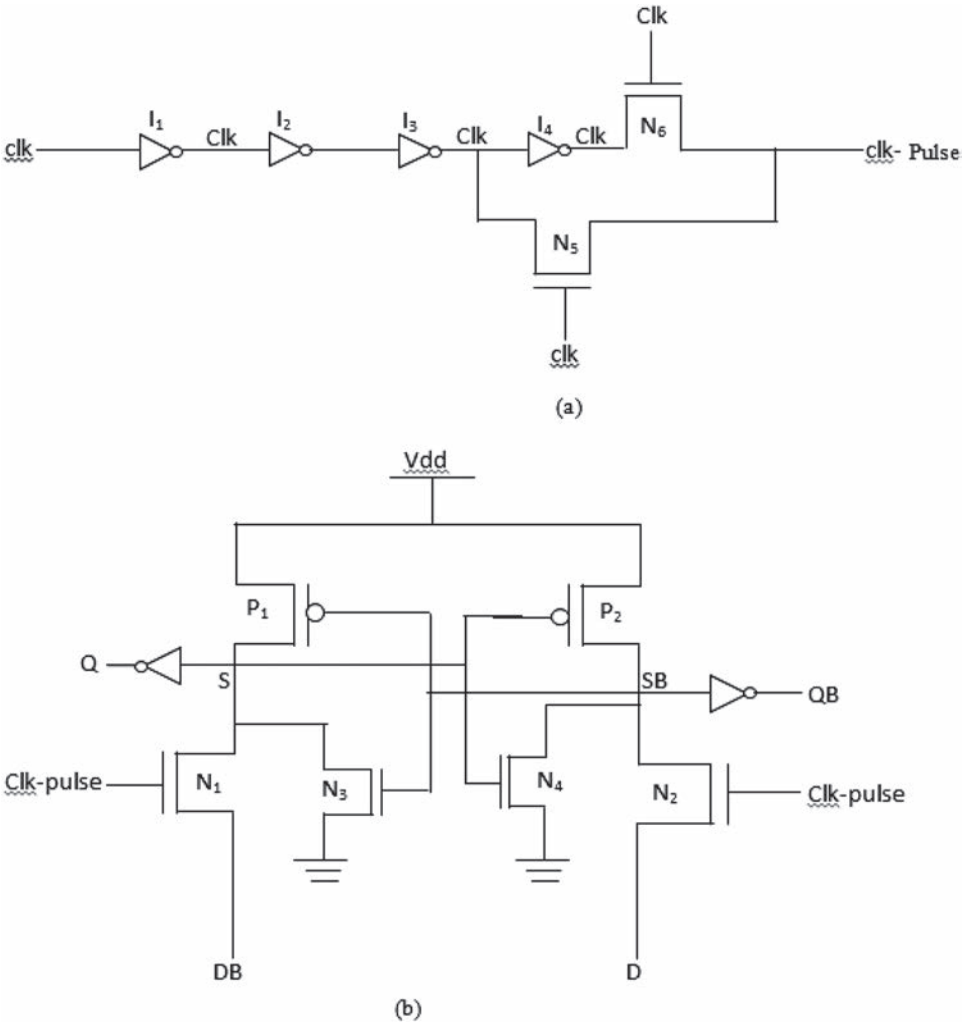

Fig. 2. Schematic diagram of DETSPF (a) dual pulse generator (b) static latch.

state D during the remaining transparent time. SB and RB transmit the signal directly into the LP1 and LP2 pull-up transistors. Data source (D) and inverted source (DB) are fed straight to transistor LN1 and LN2 operated NMOS transistors. Pull up transistors and transfer transistors are used to charge the output node Q and QB. If the flip flop is not visible, the previous value is still maintained using LP3, LP4, LN ltd3, and LN4 internal transistors. Although the data change operation is minimal, the dual pulse generator causes an unwanted clock pulse. As a result, in low switching operations, DETSAFF absorbs more power.

2.5. Clock Gated Sense Amplifier Flip-Flop

In Figure 5 you can view the clock-driven pulse generator [3, 15]. The comparator is here a significant source for both X and Y signals. Differential inputs D and DB are the comparator inputs. As power signals the buffered outputs Q1 and QB1 are. Both (X & Y) signals have respectively been introduced into the CN3 and CN4 doors. If D differs from the Q output, the X node signal is high and the Y node signal is low. The NMOS transistor CN3 is activated and a clock sign is sent to CL via CN3. As a gated clock, CL is titled. AT simultaneously generates an inverted CLK1 clock signal inserted into the CN6 passenger transistor as well as a CLK3 delay gated clock inserted into the CP6 pass junction transistor. These 2 indicators (CLK1 and CLK3) serve as a gate control signal (TG).

The signal for the TG input is the CL clock). At the up and down edge of the clock the pulse is produced. In the next n iterations, when input D is still the same, the X is pulled down near to the ground and Y to high. Thus, the CN3 junction transistor is disabled and the input pulse of clock is not transferred to CL. The CL is drawn down to the ground via CN4. The clock signal is finally blocked and the flip flop remains invisible. In Figure 6 is presented the schematic diagram of the Clock Gated Sense Amplifier flip flop (CG-SAFF). The detection stage is identical to DET-SAFF. The main alteration among DET-SAFF [6]

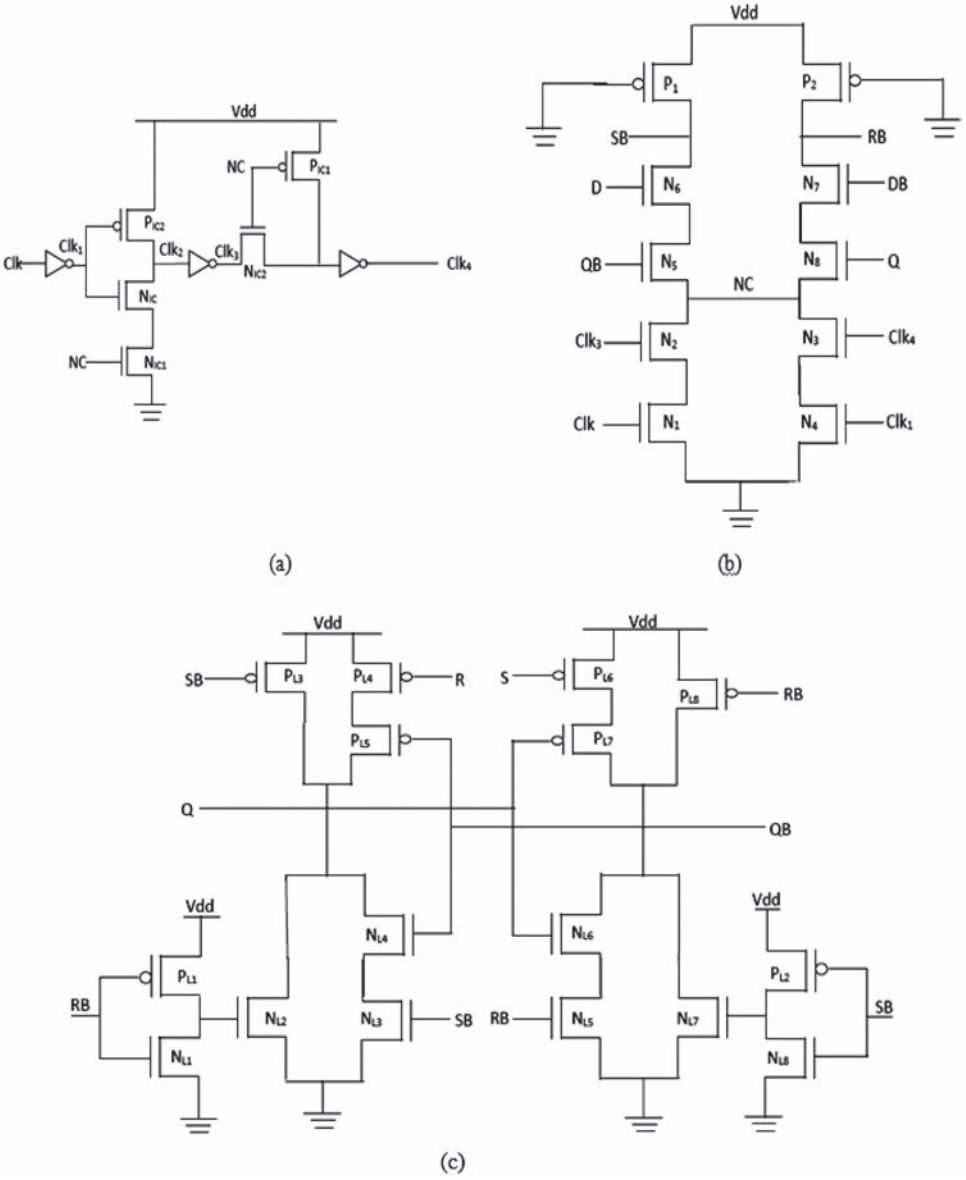

Fig. 3. Schematic diagram of ACSAFF (a) adaptive clocking inverter chain (b) front end sensing stage (C) latch.

and CG-SAFF in the latching phase is the former requirement of pulses but no pulse signal is needed in the latter phase. The buffers are created with differential outputs Q1 and QB1, used to create X and Y rather than Q and QB.

3. PROPOSED METHOD TO REDUCE POWER LEAKAGE

3.1. Sleep Method

This paper deals with CGSAFF's suggestion for a new sleep technique [9–13] to decrease leakage and complex dissipation. High-threshold transistors in the sleeping procedure are taken into consideration. The pMOS transistor sleep configuration is taken among the source power, the VDD network And a sleep transistor nMOS and pull-up mechanism between the network and the GND field. The solution planned as seen in Figure 6.

Once the electric circuit is in energetic position, the sleep transistor is activated and switched off if the circuit is inactive. This is the following. By cutting the logic circuit off from power supply and soil voltage in sleeping condition, this technique decreases the sub threshold outflow current. The transistors of sleep are sleep driven. The S and S' Signal Characteristic. The sleep signal S is kept at a logic level of 1 tension during daily activity and the supplementary sleep symbol S' at a logic level of 0 tension. The Pull down network and Pull Up Network circuit works like a conventional inverter. During the usual operations of the M1 and M2 transistors the

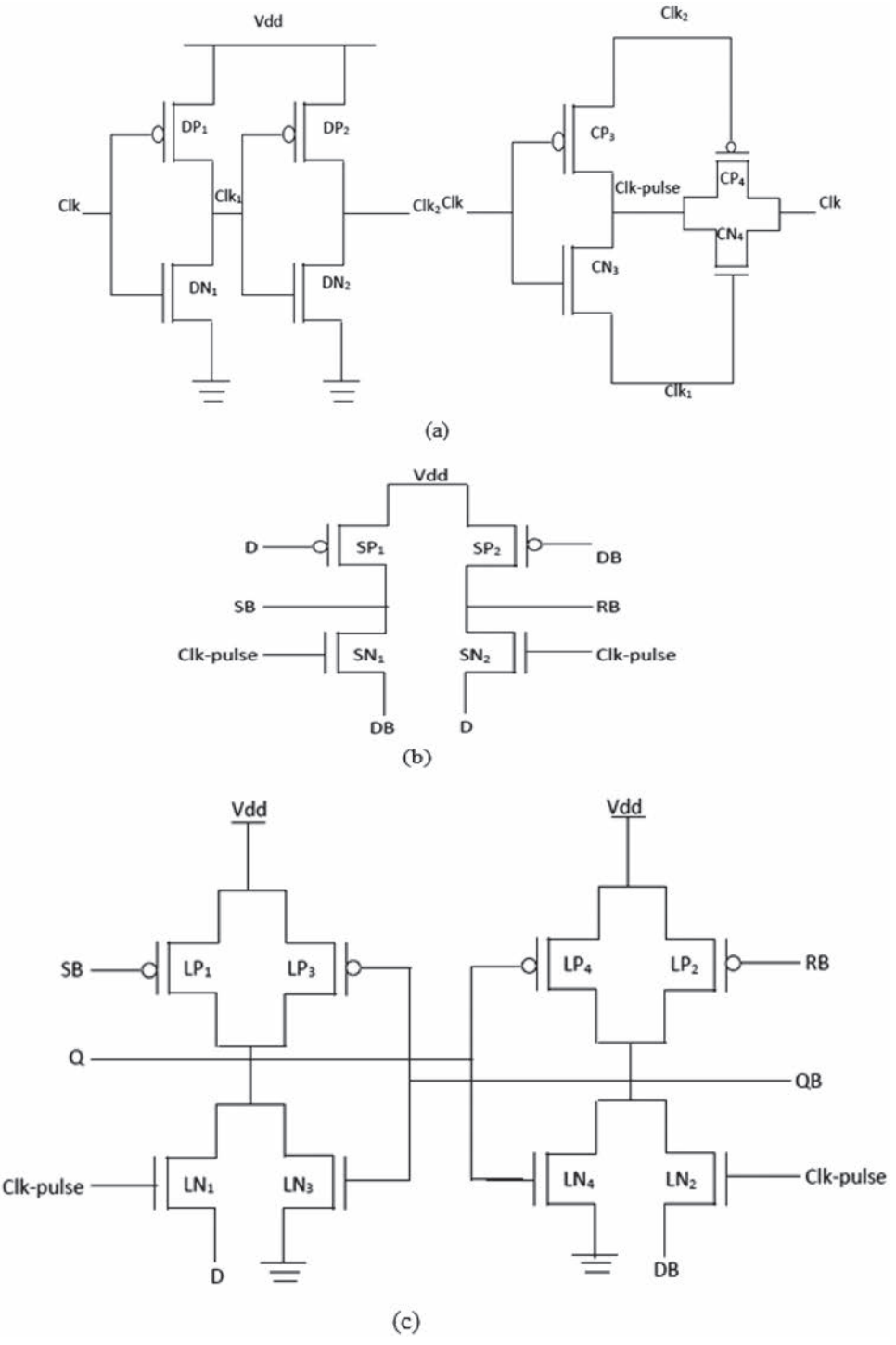

Fig. 4. Schematic diagram of DETSAFF (a) dual pulse generator (b) sensing stage (c) latch.

Virtual Vss node will also be on the ground and the Virtual Vdd node will be on Vdd. This results in reversed output by the inverter. If the inverter needs to work in standby or sleep method, the S signal will be retained at logic 0 and the S signal at logic 1 will be kept. This ensures that all networks reach a cut off condition (pull down and pull up). The virtual Vss node is therefore virtual and the Virtual Vdd node practically powerful. The inverter then enters idle mode. The theoretical Vss increases due to the cut-off M1 and M2 transistors; the possible Vdd decreases. Pull Down Network's source of body potential increases and increases Pull Down Network's threshold

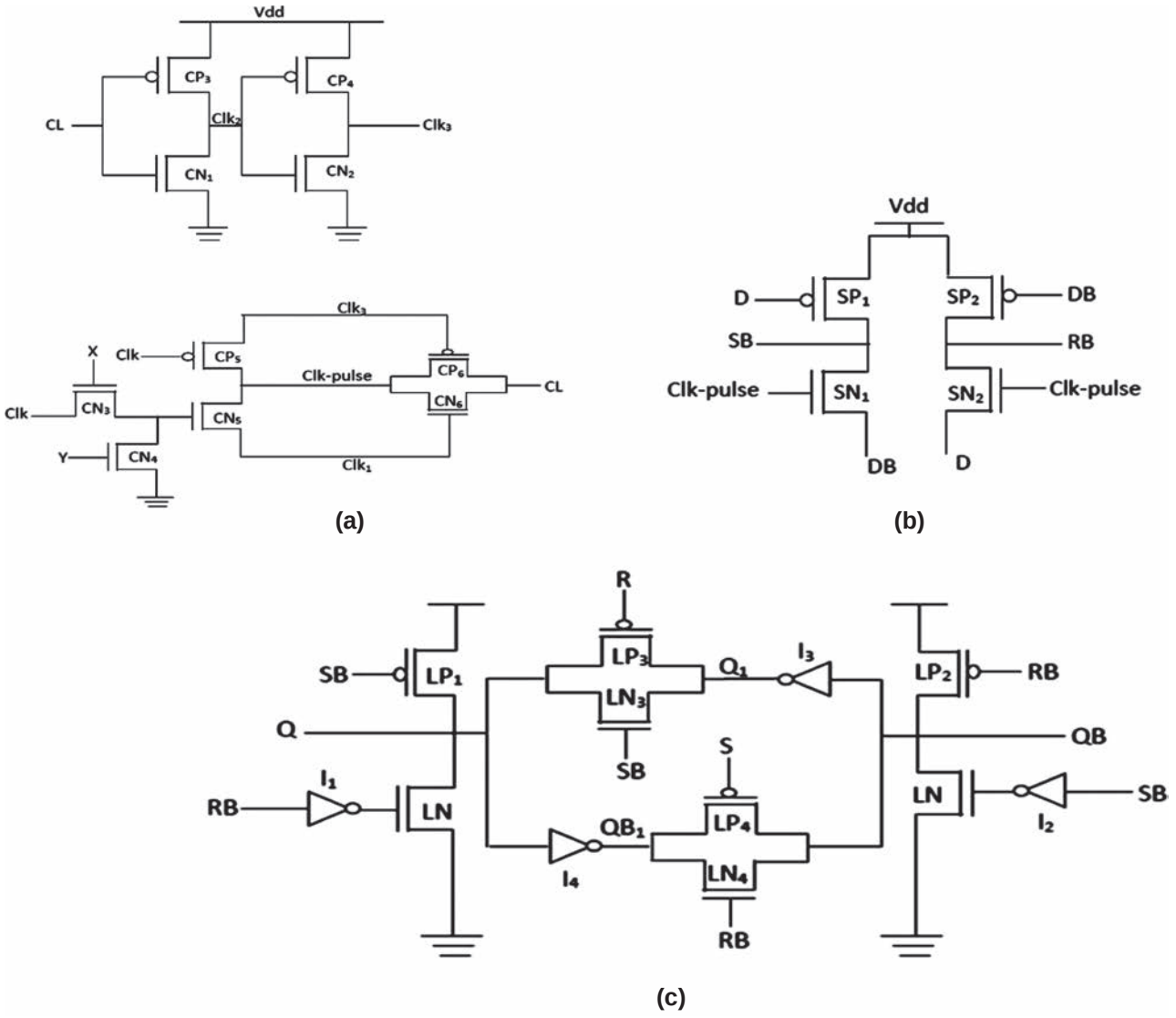

Fig. 5. Schematic diagram of CG-SAFF (a) clock-gated pulse generator (b) sensing stage (c) latching stage.

voltage. This decreases the Pull Down Network's sub-threshold current. In the Virtual Vdd and Virtual Vdd, the size of the stacked sleep transistors (W/L) defines possible stages. The sleep inverter reduces the capacity of the leakage. But it lacks state information as it goes into idle mode.

According to VLSI theory, static power is commensurate with the voltage, whereas power declines at a lower voltage. The dissipation of the leakage power in the circuit is condensed by the sleep transistor. The PMOS transistor functions as a resistance in this technology, reducing the VDD's power release to the pull up junction transistor. At the connection points between the PMOS and the Pull Up Network [17], the simulated power supply is voltages. The NMOS connects from a virtual source to the network.

3.2. Proposed System Design

In this work Clock Gated Sense Amplifier Flip-Flop (FF) has the weaker characteristics and implements the new sense-amplifier which is built using the Flip-Flop circuits with the part of sleep transistor circuit. This transistor circuit consists of different characteristic features with the higher speediness and decreased power usage. The sense-amplifier flip-flop circuit is proposed by the various sleeping factor which is implemented within the devices such as microchips, Digital Components, and the real time applications. Sleep methods are also developed to reduce power leakage dissipation. Figure 7 below shows the updated CG-SAFF design. The transistor of both PMOS and NMOS are mounted in one component of the flip-flop. Therefore, when it is not necessary and when an input adjustment for the flip-flop is not needed, the proposed clock-gating technique has been found to disconnect the switch. Dynamic

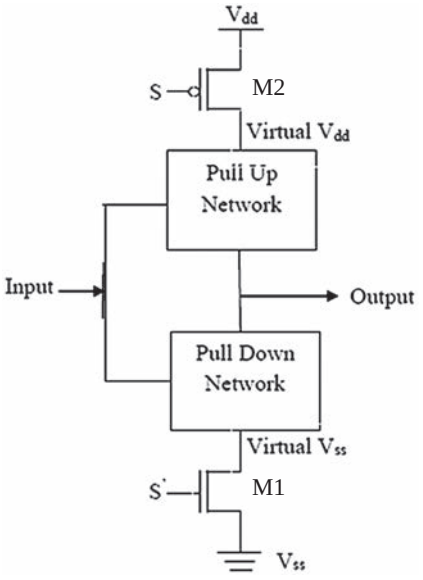

Fig. 6. Sleep approach.

power consumption can be minimised by clock gating techniques with SAFF. CG-SAFF will save up to 30 per cent of power during zero-input shifting operation using the sleep transistor. For different sequence device designs, the proposed Flip-Flop may be used. Displays Figure 8 Changed concept waveform for CG-SAFF.

To reduce the leakage power consumption, the technique proposed is indicated as CG-SAFF. This implemented technique is subjected towards the higher performance which acquires less power than the other techniques. So, the proposed technique is used in the various applications.

The proposed various stages such as the Pulse Phase, sensing and latching phase is shown in the Figures 8 and 9. The proposed technique at the sensing stage is termed as the conditional pre-charging method which is used to reduce the redundancy of the interior nodal point. By the reflection of two input points such as PMOS transistors in inbuilt in the way of nodal point. The condition is based on the nodal point that the D value remains at the higher range during the n cycles. Due to the higher range of D, SB tends to be discharged. For instance, during the $(n-1)$ cycles, the SB waveform tends to be lower where the clock pulse is higher. The RB point within the first cycle remains to be higher in the pulse region due to the pre-charged factor. The pre-charging stage is controlled with the conditional factor, pull down pathway of SB and RB region is critical with the individual one junction transistor. This transistor will decrease the settling time within the circuit. Due to the reduction in the discharging time, power will be low, delay will be minimized and therefore speed will be higher.

4. RESULT

Table I shows the influence of the power factor between CG-SAFF and modified CG-SAFF. This work is subject

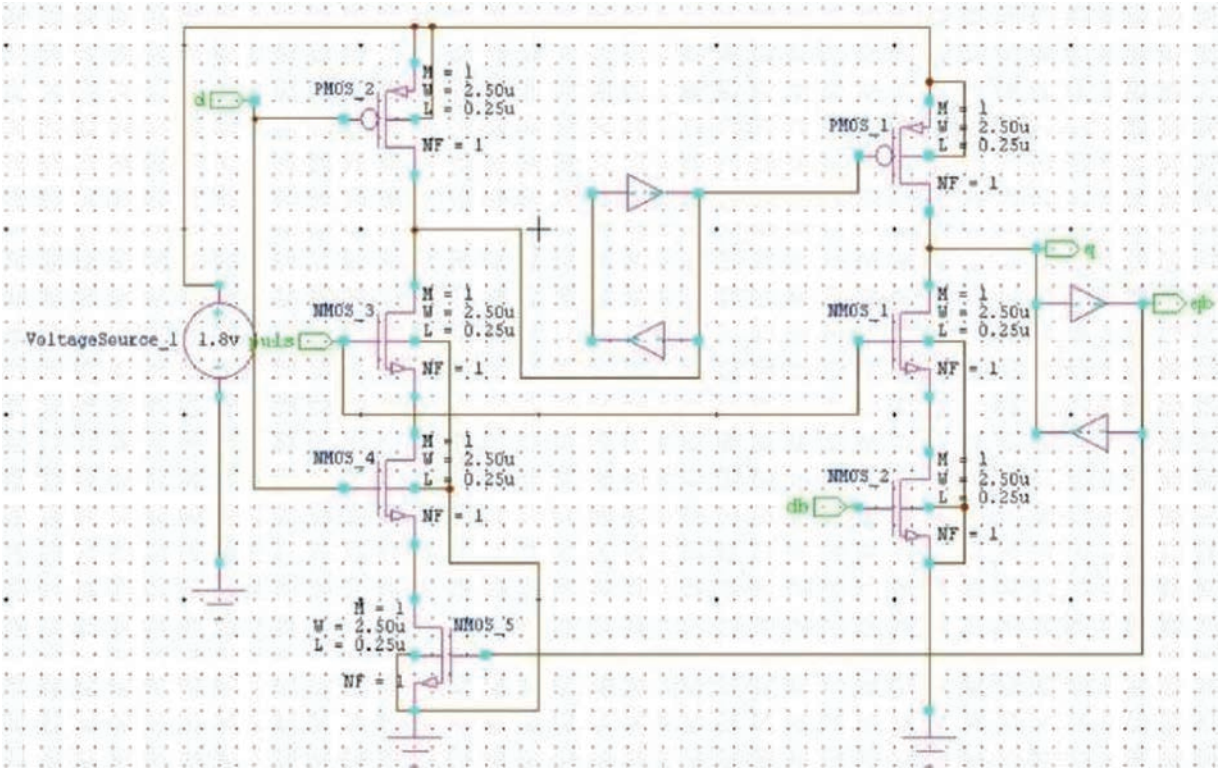

Fig. 7. Schematic diagram modified CG-SAFF.

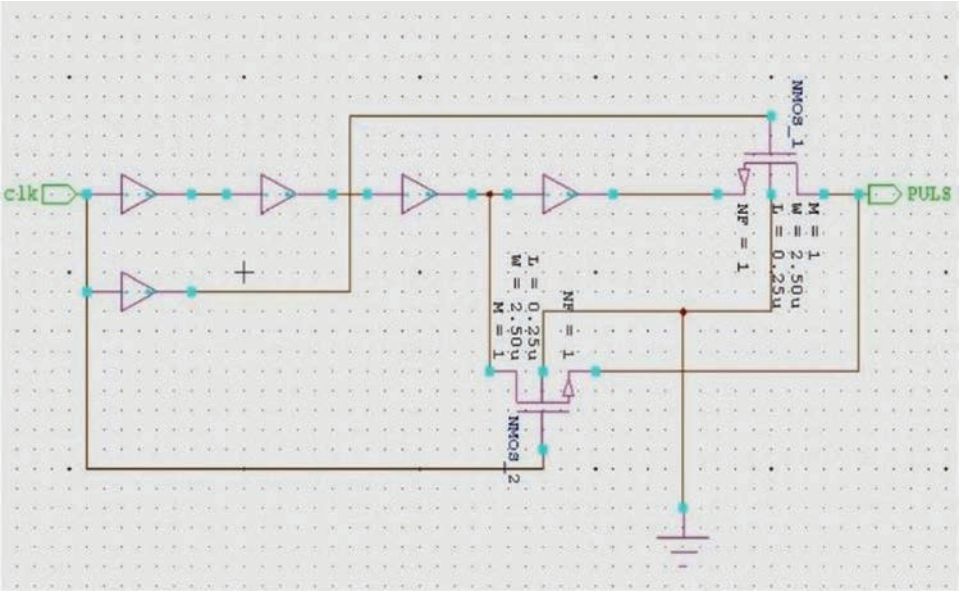

Fig. 8. Pulse phase for proposed method.

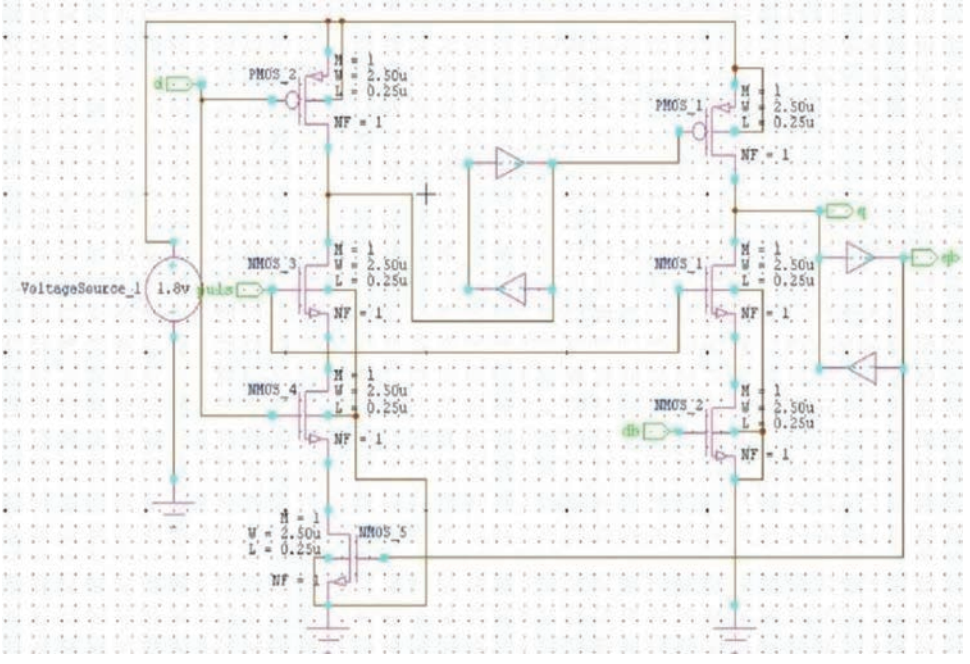

Fig. 9. Sensing and latching phase for proposed method.

to a reduction in leakage power usage in the proposed CGSAFF. CG-SAFF will save up to 30% power during the non-input shifting phase with a sleep transistor. For different sequential device architectures, the proposed flip-flop may be used.

Comparison of CG SAFF Parameter Assessment and the design proposed. For the proposed amended CG-SAFF, Figure 10 shows the output waveform. Power is lowered by up to 30 percent as opposed to the original CG-SAFF adjusted CG-SAFF. With low power operation, the adjusted CG-SAFF is better for a low power consumption. When comparing to current design, the planned CGSAFF design delay is reduced 33.34 percentage. Therefore, this current concept speed is improved here by a reduction in delay. It is derived from the data that there is a lower time lag than other FFs for the proposed MCG-SAFF. The delay was reduced by 33.34 percent. For simulation,

Table I. Influence of power factor between CG-SAFF and modified CG-SAFF.

Parameter	CG-SAFF	MCG-SAFF
Energy (mw)	79	53
Data to Q delay (Sec)	8.999	3.004
Clock to Q delay (Sec)	5.999	5.004
Number of transistors	38	36
Rise time (ps)	79.06	92.16
Fall time (ps)	78.47	91.26
MOCF (GHz)	1.25	1.25

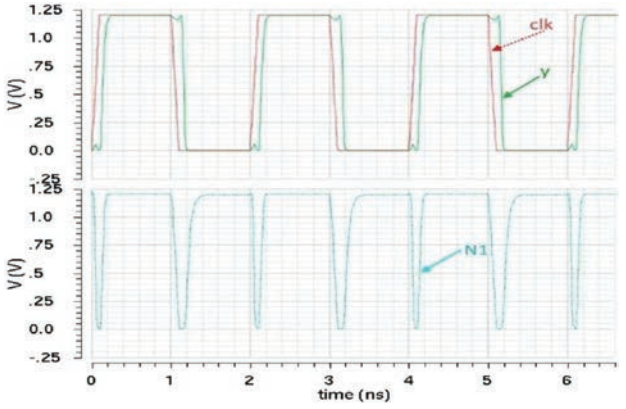

Fig. 10. Simulation waveform of modified CG-SAFF.

different test models can be used for simulating the FF designs.

5. CONCLUSION

The proposed MCGDET-SAFF is not designed directly from the basic Flip Flop design circuit. To obtain the final circuit with high efficiency in terms of low power and high speed, a stage wise improvement/modification is done on the edge triggered Flip Flop. For instance, a sense amplified Flip Flop is incorporated with the clock gating for reducing the power consumption and reducing the memory. Then it will be extended into dual edge triggered clock gated sense amplifier Flip Flop. Finally, the CGDETSAFF remains modified into MCGDET-SAFF and it can provide very less power consumption and it will increase the speed in the application.

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