A NOVEL DESIGN OF NANO ROUTER WITH HIGH SPEED CROSSBAR SCHEDULER FOR DIGITAL SYSTEMS IN QCA PARADIGM

A THESIS

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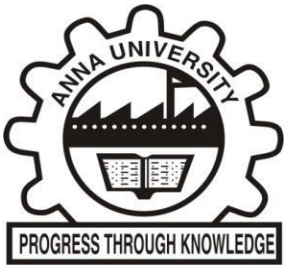

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BONAFIDE CERTIFICATE

The research work embodied in the present Thesis entitled **"A NOVEL DESIGN OF NANO ROUTER WITH HIGH SPEED CROSSBAR SCHEDULER FOR DIGITAL SYSTEMS IN QCA PARADIGM"** has been carried out in the Department of Electronics and Communication Engineering, Hindusthan College of Engineering and Technology, Coimbatore. The work reported herein is original and does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion or to any other scholar.

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ABSTRACT

The work presented in this thesis focuses on employing Quantum-dot Cellular Automata to create electronic logic circuits (QCA). The idea delves into the theory of QCA technology and terminology in depth. For a more in-depth understanding of the issue, several original concepts and implementations from the literature have been examined. It has been discovered that it is possible for novel QCA-based logic circuits and applications with enhanced circuit parameters such as area, circuit complexity, and clock delays to be designed and implemented. This motivates me to carry out the work that is part of this study program. It also includes an in-depth examination of QCA circuits and a summary of current literature in this field. The importance of researching the thesis topic has been adequately demonstrated.

It has been discussed how to create QCA-based logic circuits using a combinational technique. Implementing a QCA-based three-input XOR gate with enhanced circuit characteristics has been attempted. The combinational circuit, like a full adder and subtractor, is proposed based on three input XOR gates. This thesis considered typical circuit factors such as design complexity, speed, and power consumption when submitting novel QCA-based circuits. Before that, the low-power full adder is designed, and the performance metrics are analyzed using Multithreshold CMOS technology in various regimes.

A novel D flip-flop using the proposed QCA pulse generator has been implemented. Typically, 2-Bit and N-bit synchronous counters have

been submitted using proposed D flip-flop and pulse generator QCA circuits. The proposed circuit has been tested and analyzed their performance matrices.

A new architecture of the Nano router for high-speed data transmission has been implemented & presented in the thesis. To achieve Nano communication using the proposed circuit. The proposed course has been developed with various modules like multiplexer, demultiplexer, switch fabric, and parallel to serial converter. The newly implemented circuits have been analyzed and compared on multiple circuit parameters with their conventional counterparts. A new modular design for QCA based Nano router with various modules has been implemented in this thesis. The proposed method is a novel approach to using QCA technology for higher-order arithmetic and data transmission applications. Compared to the contemporary designs, the proposed circuit has a superior performance in terms of circuit parameters like cost, area, complexity, and power consumption.

Finally, the thesis presents a discussion of the work conducted. The results of computer simulation tests on the proposed QCA-based circuits and systems have been summarized and presented. The scope for further research in the area of concern has also been discussed. The thesis concludes with a bibliography of literature consulted during the study conducted under this research program.

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KALPANA K

TABLE OF CONTENTS

CHAPTER NO. **TITLE** **PAGE NO.**

CHAPTER NO. TITLE PAGE NO.

LIST OF TABLES

LIST OF FIGURES

FIGURE NO. **TITLE** **PAGE NO.**

FIGURE NO. **TITLE** **PAGE NO.**

LIST OF SYMBOLS AND ABBREVIATIONS

ALU	-	Arithmetic logic Unit
CPU	-	Central Processing Unit
CMOS	-	Complementary Metal Oxide Semiconductor
XNOR	-	Exclusive NOR gate
EXOR	-	Exclusive OR
XOR	-	Exclusive OR gate
HVT	-	High Threshold Voltage
HIVL	-	High-Intensity Ultraviolet Lithography
ITRS	-	International Technology Roadmap for Semiconductors
LVT	-	Low Threshold Voltage
MINs	-	Minimally Interconnected Networks
MTCMOS	-	Multithreshold Complementary Metal Oxide Semiconductor
NMOS	-	N channel MOS Transistor
PMOS	-	P channel MOS Transistor
QCA	-	Quantum-dot Cellular Automata
RTL	-	Register Transfer Level
RTD	-	Resonant Tunneling Diodes
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SET	-	Single Electron Transistor
TIEO	-	Three input Exclusive OR gate
TSPC	-	True single-phase clock
VLSI	-	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Gordon Moore predicted in 1965 that the value of transistors could be integrated into single chips that would double every 18 months. (Moore 1965) Moreover, this would occur in the early 1960s. This set of rules developed by Moore served as a baseline for semiconductor determination more than four times. The IC industry is now compelled to consider alternatives since ratings rapidly reach their fundamental limitations. It has been anticipated that the CMOS technological limit would be confined to around 5 nm to 10 nm and that this limit will be achieved as early as 2017 (Gargini, 2000) by the International Technology Roadmap for Semiconductors (ITRS). CMOS integrated circuits (ICs) are still widely used in a wide range of items in daily life, including portable electronic communications and transportation (Iwai 2008).

Increased operating frequency and decreased transistor size are seen immediately after a rise in the rating of CMOS devices. A reduction follows this in the voltage of the supply of electricity and an increase in the operating frequency. Such aggressive ratings are the outcome of a variety of wrongdoings, including presenting huge incentives and excessive levels of authority in the hands of individuals. Because of the phenomenal success of Complementary Metal-Oxide-Semiconductor circuit (CMOS) circuits, relatively inexpensive computer chips that are tiny, energy-efficient, and very

efficient are now available for purchase. However, the primary fear is that CMOS is reaching the point where it can no longer be both quick and inexpensive in its measurements. Historically, the photolithographic process used to fabricate integrated semiconductor circuits was responsible for determining the size of the features on the chip.

However, advancements in practical methods, like 193 nm immersion lithography and double patterning, have pushed the limit of 32 nm down to as low as 10 nm (Auth et al., 2012; Owa, 2014). High-intensity ultraviolet lithography (HIVL) is a promising new technology that promises smaller feature sizes (Wu & Kumar, 2007). However, because their size approaches the atomic scale, further deterioration is becoming progressively constrained due to fundamental CMOS limits. So, the size of the CMOS transistor drops as it gets closer to the source and drain, which lowers its gate electrode's capacity to regulate the voltage distribution over its channel area and the current flow through it.

The CMOS lithography-based technology is confronted with significant obstacles. Regarding power consumption, physical dimensions, leakage currents, doping ups and downs, and doping ups and downs. Researchers are exploring new choices in the nanometer layout due to the more complex and costly lithography technique. As a result, researchers are concentrating their efforts on nanotechnology as an alternative. New building materials may replace nanotechnology and CMOS in the future because of the high device density and low power consumption of these new building materials (Gargini, 2000).

In recent years, much research has been conducted employing transistor-less Nanoscale technologies to surpass current CMOS technology. Using these technologies, it is possible to attain a device density of 1012 devices/cm2 while using little power and operating at Tera frequencies in

Hertz. To do this, quantum-dot cellular automata (QCA) is a newly developed invention that is a strong contender in the research sector.

A novel method of Digital Computation and Information Transformation has been developed by (Craig Lent et al., 1993), and it looks to be a viable alternative to nanotechnology. QCA The high device density, low power consumption, and extremely fast switching speed of this technology have drawn significant interest in recent years. QCA, a revolutionary technology for nanoscale circuits that is efficient in structure and power consumption, has the potential to play a significant role in developing the next generation of computer systems. It is projected that QCA cells with a size of a few nanometers (nm) or less will be prospective contenders (Craig Lent *et al.* 1993) shortly when it comes to the size of the future.

Quantum-dot cells are the fundamental building blocks of QCA technologies and are used to create Logic Gates, Wires, and Memories. The majority gate and the inverter are the two most fundamental logic components in the QCA approach. In addition, wiring may accomplish signal propagation in the QCA Circuit. Tougaw & Lent (1994), Lent et al. 1997) Logic components may be generated by manipulating the AND, OR gates, and the majority gate. Even though the technological convention varies from that of CMOS design, it is practical and realistic for implementing low-power logic circuits. As a result, QCA is a novel breakthrough at the Nanoscale that offers an intriguing alternative to traditional CMOS technology. A possible technology for next-generation digital circuits and systems, it is frequently employed as a component of sophisticated frameworks and is becoming more commonly used.

1.2 MOTIVATION

The design of the QCA circuit differs significantly from the standard design on both the logical and physical levels, as seen in the diagram below. In addition to physical design, the emphasis is on high-end designs such as algorithms and logical design. The algorithmic method is especially significant in big systems, even though the real QCA circuit designs must handle a huge number of physical interactions that may be unwanted or disruptive in certain cases. In addition to circuit architecture and device design research, a comprehensive grasp of QCA-based nanotechnologies is required. The purpose of this thesis is to investigate the design, implementation, and power analysis of innovative logic circuits based on QCA technology.

Considering how well the QCA device performs in computing, it is vital to investigate design methodologies and demonstrations of computer arithmetic circuits that make use of the device's novel features. Many studies have been carried out in this area over the last decade, including the design of combinational and sequential logic circuits employing QCA cells, along with the identification of an optimal fabrication procedure. Because the adder, multiplier, divider, and square-rooter are the most often encountered components in an arithmetic logic unit, arithmetic circuit design is a key Subject (ALU), to make use of the characteristics of Demonstrate QCA technology and its potential advantages from a circuit design standpoint, as well as from a performance perspective, which necessitates comparisons with other circuits, particularly on large-scale designs with substantial size and complexity concerns. QCA should be used to explore both classic and innovative arithmetic circuit architectures since both are important. This is

going to happen. If large-scale designs in QCA are achievable, it would be fascinating to examine this further.

Currently, available QCA technology requires cells to be properly aligned at the Nanoscale (Tahoori *et al.* 2004) to deliver the right functionality. For QCA-based quality design, manufacturing flaws and misalignment play a critical role in determining the appropriate test for this sort of defect. Recent breakthroughs in cell creation include the self-assembly of molecules (Likharev 1987) on the surface of the substrate, which allows for the declaration of molecules on the surface of the substrate. (Qi & Sharma 2003) conducted various experiments that revealed that missing or excess cells are required for molecular implementation due to the process of cell deposition, and this was confirmed by the results. Small defects may occur as a consequence of changes to manufacturing processes' parameters. Furthermore, because of the intense cell contacts that occur when these flaws are inside or very near the target device, these defects have obvious functional consequences when they are within or very near the target device (Huang *et al.* 2004). To prevent this, testing is an imperative must. In QCA, the detection of various sorts of faults such as cell misplacement, the presence or absence of cells, and so on is accomplished.

Because of the sophisticated pipeline architecture of QCA Systems, there may be significant downsides to the QCA system as a whole. Because QCA seems to be extremely promising, it is necessary to design and develop QCA-based circuits and systems for end-users.

To carry out this study, many unique logic circuits and power analysis techniques were developed using the QCA Designer and QCA Designer E tools for QCA (Quantum Circuit Analysis). QCA has created

several energy-efficient and low-power circuits. Power analyses of low-power QCA-based circuits, as well as a demonstration of the logic circuit's implementation, have been carried out. These circuits have a distinct edge over their regular counterparts. Several intriguing characteristics of the circuit are discovered, including quick switching speed; less power usage; and a compact footprint.

1.3 OBJECTIVE AND SCOPE OF THESIS

Before this thesis, some research work has been done on QCA devices and Circuits. Some logic circuits have been designed by Tougaw & Lent (1994), Lent (1997). Preliminary work on QCA architecture has been done to understand how QCA cells work physically and later understand QCA Logical Circuit Design. For other QCA circuits, such as Multiplexers, Exclusive-OR (XOR) gate, and other QCA Logic Devices the majority of the gate was designed and studied.

Different types of wire schemes (standard, coplanar, multi-layer, and logical crossing wires) have been used to design new potential architectures for QCA. Care of the area, circuit complexity, and clock delay of these circuits are taken to reduce. The proposed TIEO (Three input Exclusive OR gate), Full adder topology evaluates the performance of different implementations QCA proposes various efficient layouts with circuits and better performance. The proposed gates can be useful in arithmetic operations, and error detection and correction circuits and phase detectors in digital circuits. Accordingly, this design has been used in various digital circuits and systems.

In QCA basic logic gates, a new three-input exclusive OR gate has been worked out. The proposed gate explores the new logic circuits with less area, less circuit complexity, and fewer clock delays. In arithmetic logic circuits, Full adders and full subtractors are the basic building blocks. The proposed gate is implemented in adder and subtractor with low complexity, ultra high speed towards a single layer.

Novel D flip-flop with pulse generator worked out and presented in this thesis. In the implementation part, an efficient sequential circuit is designed by the proposed work with minimum area and less complexity. The work is enhanced by the design of a novel nano router for high-speed data transmission with the help of a two-bit counter using a D flip-flop, multiplexer, and demultiplexer design. This proposed work explores better performance in terms of cells, area, complexity, and less power consumption.

1.4 ORGANIZATION OF THE THESIS

The thesis is planned as follows:

Chapter 1: This chapter provides an outline of the research.

Chapter 2: This chapter gives a detailed introduction to a literature review of the research conducted in the area that has been discussed.

Chapter 3: This chapter concisely describes the essentials and impressions of the QCA technology, basic QCA logic gates, clocking in QCA and types of QCA devices.

Chapter 4: This chapter explains the design, implementation, and simulation of a High-speed adder using MTCMOS technology. MTCMOS full adder was designed and the performance of the adder was analyzed in

various nanometer regimes at 90nm, 70nm, 20nm, and 180nm. In the implementation part, the array multiplier with the proposed adder was designed and their performance was analyzed in 90 nm, 70nm, 25nm, and 18nm regimes.

Chapter 5: This chapter explains the QCA one-bit full adder and full subtractor using a novel design of three input EXOR gates which takes the advantage of the QCA logic. QCA full adder and full subtractor of various existing and proposed designs stimulated using QCA designer tool. The power analysis was carried out by the QCA designer E tool. The planned adders are related in terms of cell count, latency with previously planned adder circuits.

Chapter 6: In this chapter, an original design of D type flip-flop with a pulse generator is proposed and stimulated. The various types of D Flip-flop are compared in terms of area, latency, and the number of cells used. The extension of this proposed design is to design asynchronous 2bit, 3bit, and n bit counters. The working operation of the proposed design is verified using the QCA designer tool. The various components of D-type flip-flops for existing and proposed are compared.

Chapter 7: This chapter illustrates the design and implementation of the QCA Nano router with a crossbar scheduler for high-speed data communication. This proposed design was done by the design of a 4:1 Multiplexer, 2 Bit counter, 1:4 Demultiplexer, and serial to parallel converter. The proposed design was stimulated in a QCA environment. In the comparison part, the proposed design was designed and simulated using the Xilinx environment.

Chapter 8: This chapter provides the summary and contribution of the research completed in this thesis. This is followed by a conversation on the future directions.

CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

The literature survey is concentrated on previous designs of quantum-dot cellular automata technology in VLSI at the nanoscale level. The various designs in QCA circuits in combinational and sequential designs are investigated. Also discussed and investigated a few works of Nano communication in QCA technology. In this section, the related work of the adder circuit, D flip-flop, counter, and Nano router in QCA circuits the performance matrices of several cells, area, and latency are discussed and investigated.

This review gives a far-reaching outline of existing anomaly methods by several designs and techniques. Based on the logic circuit the complex process is performed in Nano communication for high-speed data transmission. The research contribution of proposed benefits and concepts with limitations for enhancing achieve system performance and overcoming the issues and challenges that are present in the existing work.

2.2 RELATED WORK REVIEWS

The basic limit of CMOS will be reached someday if the dimensional scaling of the device is not stopped. Further scaling of existing

CMOS technology devices is hindered by the presence of short channel effects, high power dissipation, and quantum effects (Peercy & Paul 2000, Meindl & James 2003). In the existing CMOS technology, there is a scaling constraint that can be solved by emerging device technologies. The "Beyond CMOS" technologies that are being established like Single Electron Transistor (SET) (Likharev & Konstantin 1999), Quantum-dot Cellular Automata (QCA) (Lent *et al.* 1993), and Resonant Tunneling Diodes (RTD) (Chen *et al.* 1996) .

QCA is the most promising of the emerging nanotechnologies, and it is the most widely used (Peercy & Paul 2000). In contrast to conventional computing, QCA is a transistor-less computing paradigm that can attain device densities of 10^{12} devices/cm^2 and operating speeds of THz. The QCA device paradigm, which substitutes FET-based logic and makes use of quantum effects at tiny sizes, is described below. It is possible to represent binary data on cells done which no current flows and to accomplish device performance by connecting those cells (Lent *et al.* 1993, Lent, Craig *et al.* 1993).

The QCA circuits have been created and enhanced in terms of less size, less complexity, and low latency, among other characteristics. QCA technology is used to create a variety of logical devices, including adders (Hashemi *et al.* 2019, Sayedsalehi *et al.* 2011, Navi *et al.* 2010, Navi *et al.* 2009, Cho & Swartzlander 2005, Vetteth *et al.* 2002, Shams & Bayoumi 2000), sequential circuits (Xiao *et al.* 2012, Yang *et al.* 2010, Momenzadeh *et al.* 2005), memory (Walus *et al.* 2003, Ottavi *et al.* 2005), and router design (Das & Das 2012, Sardinha Luiz *et al.* 2013). Too far, researchers have investigated a variety of QCA-based circuit designs (both combinational and

sequential), including fault-tolerant QCA design (Wei *et al.* 2005), divider (Sasamal *et al.* 2016), reversible logic gates (Sasamal *et al.* 2018), and majority gate structure (Sasamal *et al.* 2018). In addition, various research has looked at well-optimized QCA designs for the Arithmetic and Logic Unit (ALU) (Sasamal *et al.* 2018 , Gadim *et al.* 2018) and have shown that they perform well. In the following adders, the binary inputs are represented by the letters A, B, and C, while the outputs are represented by the sum of the terms and carry.

QCA layout of this design employs 192 cells in 1994 and is executed in a single layer, according to the manufacturer. The notions of QCA clocking are not taken into consideration in this design. This design has been modified to include four majority gates and three inverters (Likharev, Konstantin 1999). Another version of the QCA full adder features three majority gates and two inverters, which is a variation from the previous design. This design's QCA architecture features five clocking phases and makes use of 145 cells in its QCA configuration. Full adders were designed uniquely, as seen in (Momenzadeh *et al.* 2005). An uncommon version of a majority gate with five inputs is used in this design, as is a majority gate with three inputs, one inverter, and one inverter.

There has been a proposal for a QCA layout for this design that employs three clocks and just 51 cells (Peercy, Paul 2000). When compared to (Meindl & James 2003), a changed type of this design holds two inverters at the entrance of a majority gate with five-input, rather than the one inverter that was previously provided. This design's QCA architecture includes three clock phases and makes use of 73 cells (Konstantin 1999) in its QCA configuration. In another complete adder design (Walus *et al.* 2003), which

has three majority gates and two inverters. In addition to having three clock phases and 82 cells in type-1 and 86 cells in type-2, the QCA layouts of this design include three clock phases (Walus *et al.* 2003). According to the literature cited above, complete adder gates are constructed by combining majority gates with inverters. The exclusive OR (XOR) gate, which is used in the construction of complicated digital circuits, is very important. The adder and subtractor circuits, as well as certain communication circuits such as the parity generator and checker, as well as numerous blocks in the arithmetic logic unit, are all examples of where they may be found.

QCA is one of the emerging technologies that enable great performance with minimal power consumption. QCA is a kind of quantum computing. (Berarzadeh *et al.* 2017, Singh *et al.* 2016, Bahar *et al.* 2017) provides an analysis of several QCA layout architectures for the XOR gate in the literature. The designs under consideration are based on a majority gate technique. It is common to see an XOR gate design with two or three inputs in a variety of circuit architectures. According to the authors of (Berarzadeh *et al.* 2017), they have presented an innovative and resilient XOR gate with 13 cells and an area of $0.012m^2$. In comparison to the previous designs, this one takes up less space.

The authors of (Singh *et al.* 2017) have proposed a model with 28 cells and a 0.02 m^2 surface area. It is suggested in (Waje & Dakhole 2014) with 36 cells and consumes 0.03 m^2 of space with a delay of 0.75. It makes use of two majority gates and two inverter gates and occupies 0.03 m^2 of space with a delay of 0.75. The design shown in (Poorhosseini & Hejazi, 2018) consists of 37 cells with the same area and delay as the design described in (Waje *et al.* 2014). Using 12 cells with a 0.02 m^2 area and a 1.25

delay, the authors (Bahar *et al.* 2017) establish a unique XOR gate design with a 1.25 delay. For the references, a variety of research in sequential circuit design and its QCA structures have been carried out in different ways.

The design of sequential circuits in QCA technology differs greatly from the design of sequential circuits in CMOS technology. As a result, it attracts increased interest in scientific studies. Sequential circuit designs are pipelined by nature and need a clocking scheme to function properly. Memory and flip-flop design are two very appealing areas of sequential design. Flip-flops play a critical part in the design of sequential logic circuits, which are supplemented by combinational logic circuits when needed.

Different memory design and flip-flop design structures in QCA have been presented in (Berzon & Fountain 1999, Vetteth *et al.* 2003, Yang *et al.* 2010, Dehkordi *et al.* 2011, Shamsabadi *et al.* 2009,Vankamamidi *et al.* 2008). The structural designs of QCA flip-flops include line-based, loop-based, and majority-gate-based designs, among others. Structures that are based on loop-based, line-based or majority gate structures are classified according to their level of design difficulty. (Berzon 1999, Vankamamidi 2008) are a set of structures that are based on lines. In (Vankamamidi *et al.* 2005, Taskin & Hong 2008), the loop-based structures are discussed in detail.

Five papers discuss loop-oriented QCA structures with coplanar crossover. There are certain line-based designs described in (Hashemi *et al.* 2012, Sabbaghi *et al.* 2014) that do not use the crossover approach. In (Rezaei 2018, Abutaleb 2017), a majority gate-based design of a D flip-flop is given that requires a smaller number of cells. It is described in (Goswami *et al.*

2014) how to create a multiplexer that uses flip-flops. Describe a D flip-flop design that is based on majority gate architecture.

A quantum dot cellular automaton (QCA) is only briefly discussed in the literature about networking and communication systems. Nanoscale devices, on the other hand, have recently made significant improvements, which may enable the construction of upgraded and new communication systems in the future. For example, according to the work, nanotechnology may be able to provide better in environmental, computing, sensing, actuation, radio, energy sources, memory, manufacturing, human-machine interaction, manufacturing materials and mechanics, all of which could be critical in the development of new communication systems, particularly wireless devices, in the coming years. According to the same paper, Quantum-Dot Cellular Automata is named as one of the possible technologies that force allows the making of devices that are both quicker and use less power. There have only been a few publications on QCA-based nano communication.

Many important studies in this field have been published recently, including the QCA-based data path selection presented by (Das & Das 2012), as well as the QCA-based nano routers described by both (Silva *et al.* 2015) and (Sardinha *et al.* 2013). In (Tehrani *et al.* 2011) presented a new multistage interconnection network (MIN) for use in QCA technology, which is a novel multistage interconnection network. Diverse minimally interconnected networks (MINs), such as the omega network, the butterfly network, the baseline network, and the generalized cube network, were proposed, and it was demonstrated that the QCA-based design outperformed other

nanotechnology-based implementations such as the complementary metal-oxide-semiconductor and the carbon nanotube field-effect transistor.

In addition, the wire-crossing network, also known as the cross-bar network in QCA, was suggested by (Graunke 2005), and it makes use of time-dependent latching devices, shift registers, parallel-to-serial converters and to accomplish its goal of high performance. Finally, (Tougaw & Khatun 2013) advocated the use of QCA to create a "scalable signal distribution network". An unlimited number of combinational functions may be used to distribute a set of N inputs to an arbitrary number of outputs.

This is the basic purpose of this network. (Tougaw & Khatun 2013) Proposes an architecture, that is much delayed and efficient since it uses just four clock signals regardless of the number of inputs it receives. (Das *et al.* 2016) Presents the suggested design of a QCA-based reversible Nano router circuit, which is fully novel in both the QCA and the reversible domains. Architecture for a high-speed crossbar scheduler with improved efficiency is provided and stimulated in this research study utilizing the QCA designer tool.

Several different router designs based on QCA technology have been considered as possible references. The majority of gate-based data selector cum router circuit suggested in Das & Das (2012) is described in detail. Sardinha Luiz (2013) describes a novel router architecture that was obtained at the receiver side with the use of a demultiplexer and a parallel to serial converter. An advanced multilayer crossover is used in this design. Iqbal *et al.* (2013), Shin *et al.* (2014) suggest several different QCA layouts

for various modules in the router architecture, such as multiplexers, demultiplexers, and wire crossing mechanisms.

Das *et al.* (2016) describes the use of a reversible gate to accomplish Nano communication. QCA technology is used to construct an efficient multiplexer for crossbar arbiter designs, as suggested in (Thakur *et al.* 2016) for crossbar arbiter design. The on-chip crossbar scheduler, which has been suggested and implemented in (Thakur *et al.* 2018), may be used for high-speed applications.

Implementation and comparison of the suggested structure may be done using either the CMOS or the QCA technologies. This paper presents the reversible logic with a space-efficient Nano router (see (Kamaraj *et al.* 2020)). Using a multilayer cross-over structure, this research article was completed.

2.3 SUMMARY

One can see that a research trip begins with an investigation of the Literature Review or a survey and concludes with a comprehensive understanding of the proposed work, its techniques, and its findings. The results of a successful Literature Survey assist the writers in refining, refocusing the issue, or even changing the subject depending on the circumstances. As a result, this literature review provides an evaluation of a body of research that answers the study topic and sheds insight on the future implications of our difficulties. The phase or process of literature study is recursive since the more we do, the more information we acquire.

This chapter-2 provides a clear perspective of the current methodologies as well as how projected performance is supported by the Literature Review presented in this chapter.

CHAPTER 3

QCA TERMINOLOGY

3.1 INTRODUCTION

QCA cells interact in a columbic manner, in which surrounding cells impact the polarization of each other. This chapter discusses the most important parts of QCA theory as well as related subjects. Review of the QCA Logic Gates at the Fundamental Level the terms "Majority Gate" and "Inverter" are introduced, which represent the fundamental building blocks of any QCA circuit design. QCA is used to explain the implementation of fundamental logic gates, such as AND, OR, NAND, and NOR, to get a better grasp of technology.

The fundamental design concepts that are implemented in QCA circuits are addressed. The QCA paradigm goes into great length on the significance of the clock in particular. This section illustrates the history of the QCA device, including QCA cells, clocking, basic logic, and gates. The provision of rising Nano logic gadgets is made available. The fundamental pattern schemes and model engines for quality control are shown.

3.2 QCA CELL

To carry out Boolean logic operations, Quantum Dot Cellular Automata (QCA) is a nanostructure model that makes use of the quantum dot range to carry out the task. Narrow semiconductor (or) metal islands with a

width lesser adequate to deliver charging energy greater than –BT (where T is the operating temperature and B is Boltzmann's constant) is known as quantum dots. A QCA cell may be thought of as a group of four quantum dots that are place at the corners of a square and are each loaded with two free electrons that can tunnel through the dots in the vicinity of the center of the square. Because of Coulomb repulsion, the free electrons are placed on distinct dots at various sides of the cells to extend their position by quantum automatically. With four sides, there are two viable arrangements allowing binary logic to operate. As seen in Figure 3.1, two bistable states arise in the diffusion of p-+1 and p=1. When the division of one cell is gradually switched from one condition to another, In QCA cell, the circulation of the second cell exhibits a highly bistable shifting of its circulation. The Schrodinger formula, which is based on quantum mechanics, is used to set the conductivity of electrons within a QCA cell.

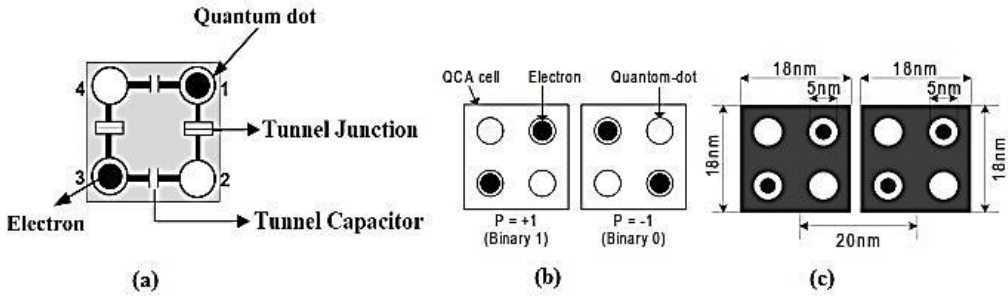


Figure 3.1 QCA cell (a) Structure of QCA cell (b) Two different polarization (c) Dimension of QCA cell

The polarization “P” of electrons can be described as:

$$P = \frac{(\rho 1+\rho 3)-(\rho 2+\rho 4)}{(\rho 1+\rho 2+\rho 3+\rho 4)} \tag{3.1}$$

where, ρ_i is the anticipated charge value on the Dot. In the absence of an electron, the expected value of charge on a quantum dot is "0." There are just

two potential values for polarisation P in the traditional concept: -1 and +1. If electrons are diagonally oriented on the left side of a QCA cell, then the polarisation of the cell is thought to be -1, and the QCA cell is in state low or logic '0'. If electrons are diagonally oriented on a QCA cell's right side, the cell's polarisation is regarded as being positive (or logic "1"), and the QCA cell is in state high or logic "1".

3.3 QCA CLOCKING

A QCA circuit's primary architectural characteristic is its clocking. Along with directing data flow, it also delivers power gain and lowers power dissipation. Clocking is used on the circuit in QCA technology for the following reasons:

- Timing control: Since clocked cells relax more quickly than unclocked cells, the clock signal is the only instrument available to control the timing of QCA circuits and to ensure quick switching of the cell state.
- Control of information flow: Since there is no current flow in QCA, the direction of information flow from the input cell to the output cell is controlled by the clock signal.
- Since the net energy change in the QCA system for one clock period could be stated as, it is possible to return the lost signal energy to the environment by

  Enet = Ein +Eclock +Eout + Ediss

where Enet denotes the overall change in energy, Ein denotes the energy of the driving cell (input cell), Eout denotes the energy used by the output cell, and Ediss denotes the energy lost during the signal path. Therefore, Eclock is necessary to make up for the energy lost along the way in order to guarantee a net energy change of zero.

- Forcing the circuit to stay in the quantum mechanics ground state, this is very important to achieve proper working of a QCA system.

To manage the interdot tunneling barrier of the QCA cell, which is responsible for the adiabatic change, a many-stage clock is used in QCA. The cells are divided into channeled sections (Lent & Tougaw 1997, Hennessy & Lent, 2001, Craig *et al.* 2006) by their mutual classification. This timing plan allows a zone of cells to carry out an estimate and maintain its current state by lowering the interdot barriers between them.

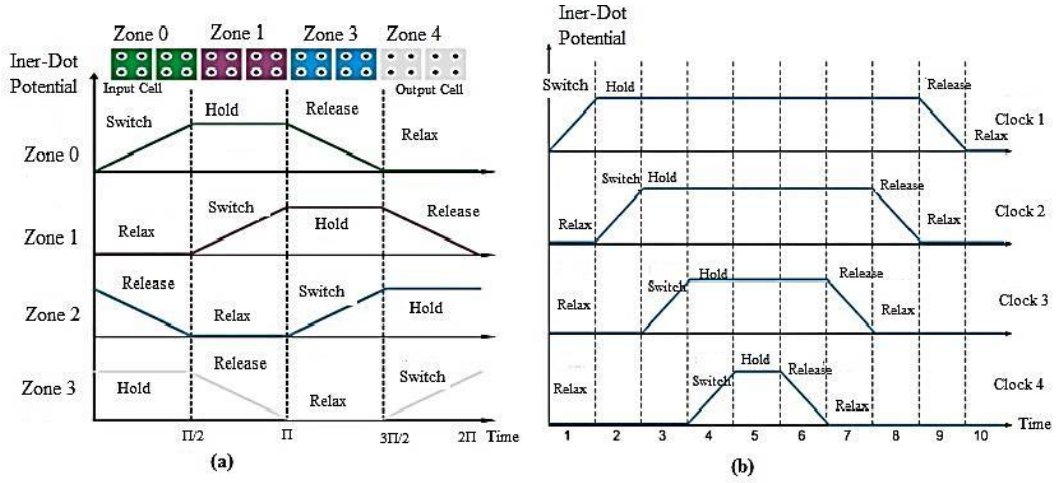


Figure 3.2 QCA clocking (a) Four phases of clocking zones (b) Bennett clock waveform

Switch, hold, release, and relax are the four clock phases seen in Figure 3.2, and they are used in the following ways: Interdot potential bars are decreased during the switch phase by providing an input signal, and data multiplication is achieved by electron tunneling during the switch phase. By gradually raising the barriers, the cell can maintain its polarization and the output of the array may be used as input to the next level of the array. During the release and relaxation phases, the QCA cell begins to thin its diffusion by lowering the barriers, allowing them to maintain its polarized state of affairs.

The purpose of this kind of clocking carrier is to increase the self-closing in the QCA.

3.4 FUNDAMENTAL LOGIC AND GATE

Among the most important QCA components are the QCA wire, the inverter, and the majority gate. By forming coulomb alliances between cells, the binary rate diffuses from the input to the output. The wire formed by transmitting cells might be an even row or it could be made up of cells that have been rotated 45-degree, rather than in the usual 90-degree orientation. Apart from that, QCA cells fix not need to be in a straight line with one another to convey binary indications effectively. Figure 3.3 shows how cells with a 90-degree adjustment may be placed adjacent to an off-center group.

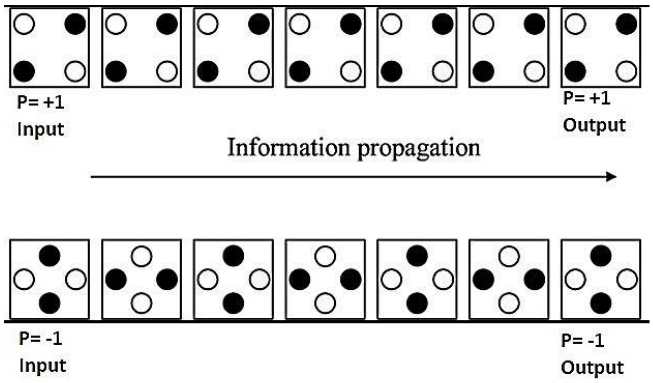


Figure 3.3 QCA wires

As seen in Figure 3.4, an inverter may be constructed by attaching cells at a 45-degree angle to one another, resulting in the generation of opposing polarization. In Figure 3.5, a three-input majority gate, which is a fundamental QCA logic function, is shown. A majority gate is represented by the logic formula M(A, B, C)=AB+BC+CA. Majority gate based AND, Majority gate based OR gates may be implemented as shown in Figure 3.6 by setting one of the inputs to logic 0 or logic 1 and the other to logic 0.

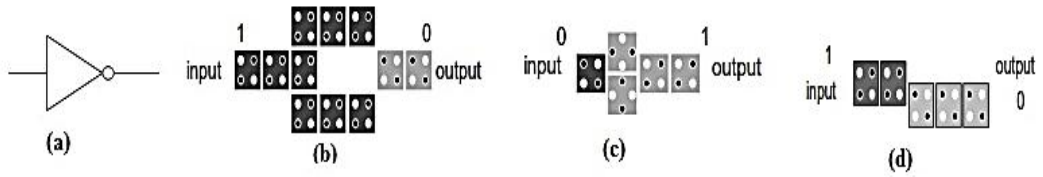


Figure 3.4 QCA Inverter (a) Symbol (b) Various QCA structures

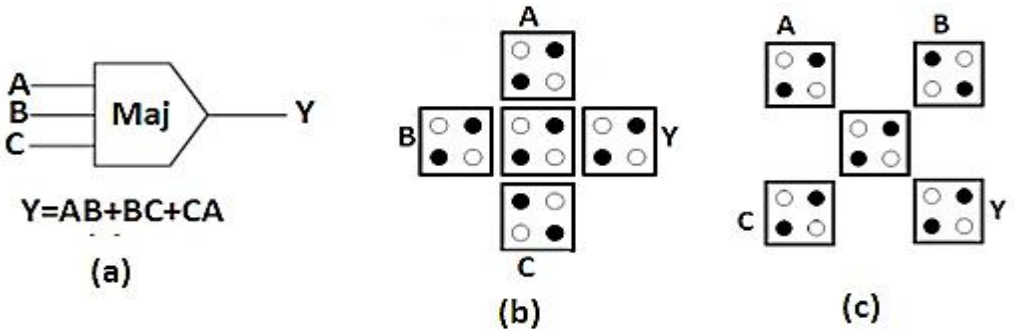


Figure 3.5 QCA Majority Gate (a) Symbol (b) OMG (Originally Majority Gate) (c)RMG (Rotated Majority Gate)

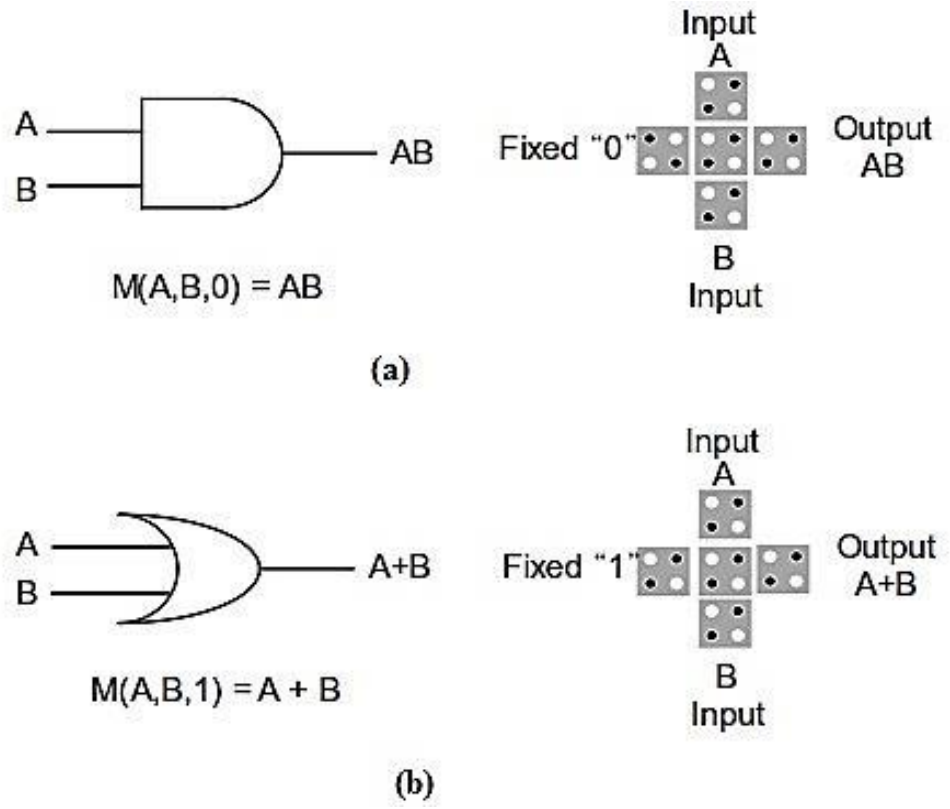


Figure 3.6 QCA Gate (a) Symbol and QCA layout for AND gate (b) Symbol and QCA layout for OR gate

3.5 QCA WIRE CROSSING

There are three types of wire crossing in QCA: Coplanar wire “Cross orders”, multilayer Crossovers, and logical crossover.

3.5.1 Coplanar Wire Crossing

It is possible to create coplanar crossing utilizing 45-degree and 90-degree QCA cells in one layer of QCA cells, with each QCA cell allocated to one side of the crossing. These cells can travel across crossings without having any meaningful impact on one another. Figure 3.7 (a) depicts a crossover mechanism with a single layer. There are only straight cells (non-rotating) in the first wire, and only moving cells (rotating) in the second. According to the finding from coplanar wire crossing that when 45-degree and 90-degree cells are put in a row, their positions do not interfere with one another. The orientation of two wires is orthogonal to one another.

This results in coupling between two 90-degree cells at the junction, even though they are just one cell apart in space. According to some reports, this coupling is weaker in a normal wire, and the ensuing crossover is less likely to be observed as a consequence. This efficient coplanar Wire crossing has become immensely popular because it is a never-before-seen occurrence that was presented by QCA.

Although it has fewer robustness concerns and building challenges (Shin *et al.* 2013), it has fewer disadvantages. Because of the weak connection, the crossover is very sensitive to physical characteristics like cell size, inter-cellular spacing, temperature, and so on. Even though the physical parameters have been optimized, there are circumstances in which a circuit

with numerous crossings might behave in an unanticipated manner despite the optimization. In addition, several researchers have attempted to boost the strength of this wire crossing approach (Bhanja *et al.* 2007) by increasing the number of wires crossed.

3.5.2 Multi-layer Wire Crossing

As illustrated in Figure 3.7 (b), a multilayer wire crossover, either 45-degree or 90-degree crossing the cell, is transferred to the second layer after passing through the crossing. After passing through the crossing, the wire returns to the original layer. The positioning of QCA cells in many layers allows for multi-layer wire crossing to be performed. In the second layer, the multi-layer strategy crossing will be performed, and it can be applied to the vertical distance between two wires of the same cell type to prevent the signal from leaking from one layer to another between the wires and between the wires and between the wires and between the wires and between the wires.

It is possible to create cells that are layered between levels. The application of numerous active QCA layers on top of each other is necessitated by the use of this approach. Improved simulation results, as well as smooth operation, are obtained with multi-layer Crossover. The data transfer is dependable (Gin *et al.* 1999).

3.5.3 Logical Wire Crossing

It is based on the interference of clock phases on each other (Bernstein 2003) that the logical crossing technique is used, and it only employs one kind of QCA cell. This technique is used "Cells in the Switch phase may cross over into cells in the release phase and cells in the hold

phase. Cells in the resting phase can communicate with one another without polarizing each other "..... It is necessary for the input cell at the crossing to have a phase difference of at least one-half cycle. This is the primary limitation that the suggested crossing technique puts on the circuit design. In a nutshell, when the wires are crossed, there should be a 180-degree phase difference between each of the wires. Figure 3.7 (c) depicts a diagram of the logical wire crossing technique. It is worth noting that logical crossover is the most attainable of the approaches discussed here. One of the most significant requirements for a functional QCA Circuit is its robustness, minimal circuit overhead when utilizing just one kind of cell, and compatibility with single-layer design.

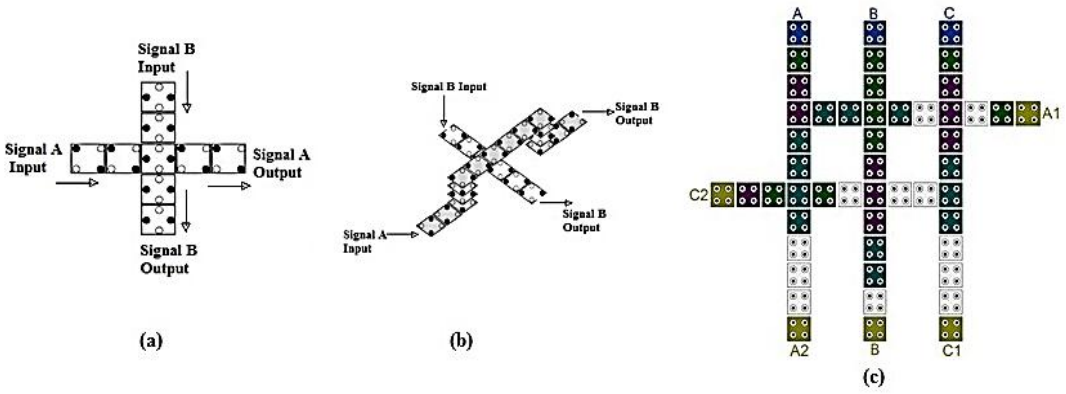


Figure 3.7 QCA wire crossing (a) Coplanar (b) Multilayer (c) Logical

3.6 QCA IMPLEMENTATIONS

Three types of QCA implementations are

- Metal QCA
- Molecular QCA
- Magnetic QCA

In this part, the investigational implementation of all of the above methods is discussed.

3.6.1 Metal QCA

The metal QCA application is the first execution to share the operation of QCA cells, and it is the first execution to do so. This technique is comprised of metallic tunnel junctions and small capacitors, among other components. This gadget is made up of four Aluminum islands (dots) that are connected with aluminum oxide.

Figure 3.8 depicts the construction, which includes a tunnel junction and a capacitor made of metal QCA. The island capacitance of the device, which is dependent on the area of the tunnel function, is responsible for determining the waving temperature of the device. Metal islands with dimensions of one millimeter have been used in this experiment. Because of the size of the island, metal island plans are retained at very low heats to investigate quantum phenomena (Toth & Lent 1999).

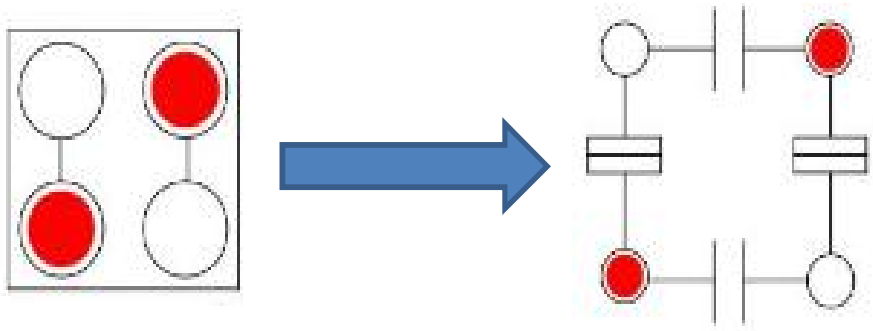


Figure 3.8 Metal dot QCA cell

3.6.2 Molecular QCA

The Molecular QCA application offers advantages over the other executions in that it operates more efficiently and performs better at room temperature than the others. The cells in molecular QCA are physically identical to one another at the atomic level. In the presence of redox centers, every molecule functions as a QCA cell (Lent *et al.* 2003, Lu *et al.* 2007). With charge configuration, the data is computed in these dots, and the tunneling is provided by ligands that bridge the gaps between the dots. One possible use for a QCA cell is a single molecule with charge concentrated in certain places that allow the charge to tunnel through the sites. The structure of a molecular QCA cell is seen in Figure 3.9.

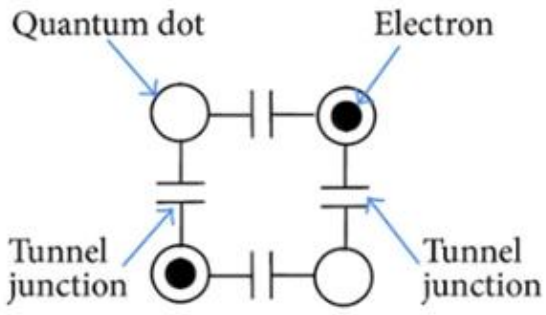


Figure 3.9 Molecular QCA cell

3.6.3 Magnetic QCA

The employment of magnetic objects in the use of QCA devices is made possible by the ease with which they can be manufactured, their resilience, their low power consumption under difficult working circumstances, and their insensitivity to radiation. When using magnetic QCA, a Nano magnet is used as the main cell. To perform computing, the magnetic cells are static in a network-like arrangement. To period, the Nano

magnets have been showed to achieve at room temperature on a preliminary basis. On the other hand, it has been shown that if 10^{10} of the Nano magnets flip 108 times per second, the magnets squander is 0.1W of power (Imre *et al.* 2006).

3.7 SIMULATION TOOL

A variety of software packages, including QCA Designer Ver 2.0.3 (Walus 2004), QCA Designer-E (Sill *et al.* 2018), and QCA Pro Tools (Srivastava *et al.* 2011), are available for analyzing QCA circuits, confirming circuit operation, and estimating dissipated energy. QCA Designer is a simulation tool that is used to develop layouts and run simulations of the QCA architecture for circuit design.

The tool makes it possible to describe the many components of a digital design in detail. This tool also enables the definition of clock zones for the design to be used in the development. One additional specific simulation engine is offered in the QCA Designer-E tool for the computation of energy dissipation in electron volts (eV), and it is known as the Coherence vector energy engine (with Energy). Calculating the energy dissipation of QCA circuits is made easier with the aid of this tool. This tool, known as QCA Pro, is a probabilistic modeling tool that is used to predict error and power dissipation in the design of QCA circuits.

It takes as an input the layout file created by the program QCA Designer and displays it on the screen. Other design factors, such as temperature and kink energy, may be specified by the design requirements. Additionally, the tool may be used to estimate polarization Error in each QCA cell for a certain input vector, in addition to assisting with Quick Check of

QCA circuit design (see below). In addition, the QCA Pro tool calculates the average, maximum, and lowest power dissipation in a QCA circuit when non-adiabatic switching is used. The energy dissipation of the suggested circuit is investigated in this paper utilizing the QCADesigner-E tool.

Using this tool, you can figure out how much energy is being dissipated by a QCA circuit. Included in this tool are three distinct simulation engine settings, which are the coherence vector, the coherence vector (with energy), and the bistable approximation, all of which may be used simultaneously. It is possible to determine both the power and energy of a QCA cell by utilizing a Hamiltonian matrix, which may be expressed in Equation 3.2 for a two-state system.

$$H = \sum_j \begin{bmatrix} -\frac{1}{2} P_j E_{i,j}^k & -\gamma_i \\ -\gamma_i & \frac{1}{2} P_j E_{i,j}^k \end{bmatrix} \tag{3.2}$$

3.8 SUMMARY

This chapter gives an overview of fundamental QCA technology, which will aid in the development of a solid basis for the research effort now under consideration. I attempted to cover quickly convey the progressive evolution of research from its most fundamental level, using the most recent QCA model. In this foundational chapter, the author shows how to design and implement fundamental logic devices utilizing quantum-dot cellular automata (QCA), such as AND, OR, and XOR gates, as well as how to wire them together.

In this chapter, you will learn about the model rules, the latest quantum-dot cellular automata (QCA) device design, and the available clock functions. It is offered a detailed explanation of wire crossing using QCA as an example. The procedure of the clock has been shown in detail. It is a critical component of the QCA circuit. This chapter also includes a short overview of the simulation tools, and it is determined that the QCADesigner and QCADesigner E, as well as the QCAPro tools, are being utilized for the computer simulation of the QCA circuit within the scope of this study.

CHAPTER 4

DESIGN AND PERFORMANCE ANALYSIS OF LOW POWER HIGH-SPEED ADDER AND MULTIPLIER USING MTCMOS IN 90 NM, 70NM, 25NM AND 18NM REGIME

4.1 SCOPE AND OBJECTIVE

One of the most significant components of a digital processor, CPU (Central Processing Unit), and ALU (Arithmetic and Logical Unit) is the adder. VLSI circuits with smaller footprints and lower power consumption are required for portable devices such as cellular phones, personal computers, and personal digital assistants.

As a consequence, the design of a low-power, high-speed adder is very beneficial and essential (Dan Wang *et al.* 2009). Static adders in digital logic circuits have concerns with leaking power and speed, which are both undesirable. To address these challenges, dynamic adders with low power consumption and fast speed are commonly used. In this study, the goal is to minimize leakage power and current in a one-bit full adder with a small number of transistors by using MTCMOS (Multi threshold Complementary Metal Oxide Semiconductor) technology.

4.2 RESEARCH METHODOLOGY

When designing CMOS logic circuits, to employ a greater number of transistors than usual. As a result, the static power consumption, leakage

current, leakage power, and die area all rise in proportion to the increase in die area. With the use of dynamic logic circuits with lower die area consumption, as well as a decrease in leakage current, it is possible to achieve a minimum delay (Rastogi & Pandey 2015).

In the dynamic logic circuits discussed in (Rakhi et *al.* 2012, Sivakumar et *al.* 2013), new technologies such as domino logic, TSPC (True single-phase clock), and MTCMOS (Multi threshold Complementary Metal Oxide Semiconductor) has been introduced to replace older technologies. The decrease of leakage power in VLSI circuits is critical in deep submicron technology, where it plays a significant role in circuit design. There are a variety of strategies (Song Yang *et al.* 2007) that may be used to reduce sub-threshold leakage power in dynamic logic circuits, including dual-threshold techniques for critical routes and multi-threshold techniques for non-critical paths.

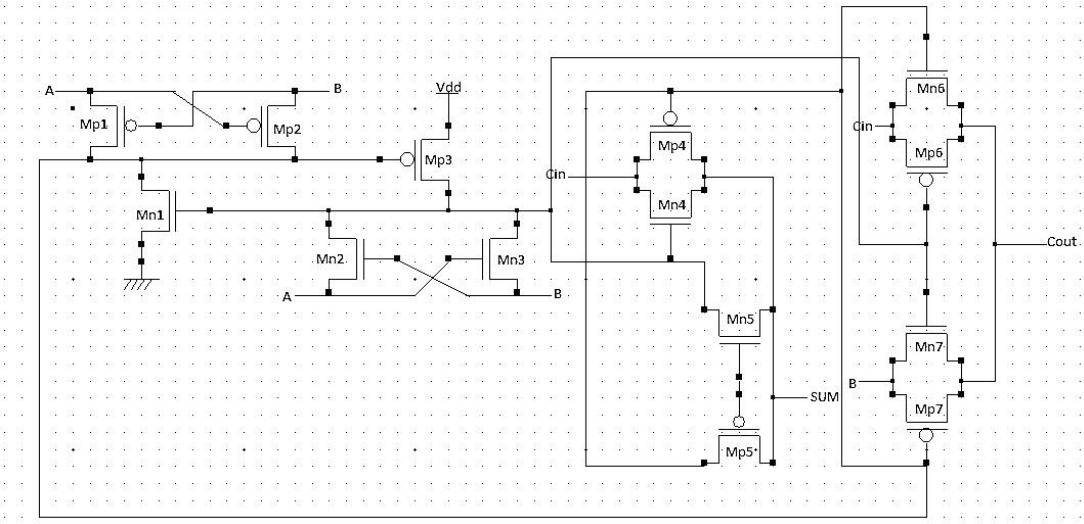
To reduce leakage power in low-power designs, two effective approaches are described in (Paanshul Dobriyal *et al.* 2013), namely multi-threshold voltage CMOS and voltage scaling methodology. In MTCMOS technology, high Vt (HVT) transistors are used in circuitry, whereas low Vt (LVT) transistors are used in circuitry. Sleep transistors are the technical term for these transistors. Ordinarily, a header or footer of PMOS for HVT and NMOS for LVT is put between the logical circuit and the supply or ground wire.

The sleep transistor is regulated by the control signal in both the active and standby modes. As soon as the control signal is enabled (control signal=1), the sleep transistor is turned on, and the logic circuit begins to

work in normal mode at a high rate. The control signal is disabled (control signal=0), the sleep transistor is turned off, and the logic circuits run in the idle state when the control signal is deactivated. This has the effect of considerably reducing sub-threshold leakage current with just a minor delay (Anis *et al.* 2002).

4.3 PROPOSED WORK

The present one-bit complete adder is developed in Abu-Shama & Bayoumi (1996). With 14T (14 transistors) with XNOR (Exclusive NOR gate) module and XOR Abu-Shama & Bayoumi (1996). (Exclusive OR gate) module via transmission gate, and it is implemented in with XNOR (Exclusive NOR gate) module and XOR (Exclusive OR gate) module. With the use of cross-coupled MOSFETs in this architecture, it is possible to completely remove the gateway voltage loss.



(Source: Abu-Shama & Bayoumi 1996)

Figure 4.1 Existing full adder

The most effective technique is MTCMOS. MTCMOS technique is proposed to satisfy the lower threshold voltage requirement as well as to increase the speed of the circuit. In other words to get high performance and high speed circuit.The most significant flaw in the present work is that the output of the XNOR module is used as the input of the XOR module. The design's primary benefit and disadvantage are that it has lower short circuit power dissipation and is not capable of driving larger loads. The proposed study involves the design of entire adder and multiplier circuits in several nanoscale regimes, including 90nm, 70nm, 25nm, and 18nm, employing MTCMOS technology in various nanometer regimes. Figure 4.1 depicts the circuit design for the present one-bit full adder in, which is shown in Figure 4.2 is a schematic of the layout of an existing ladder.

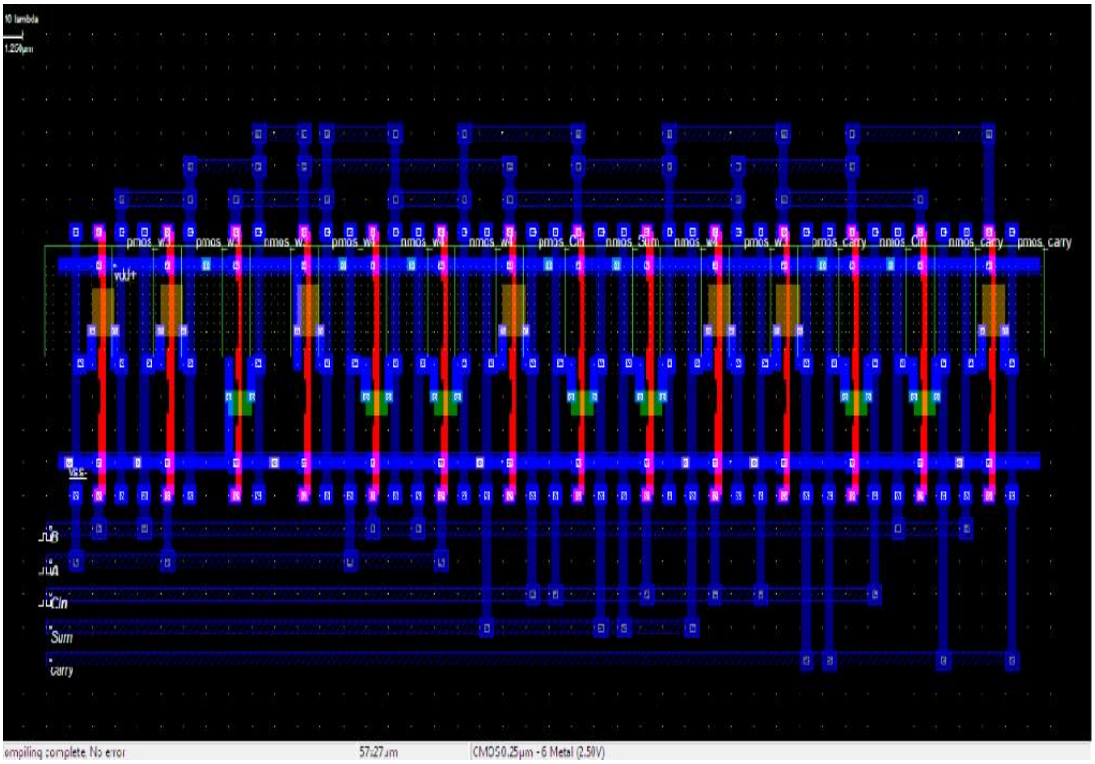


Figure 4.2 The layout of the existing full adder in 90nm technology

4.3.1 Proposed One-Bit Full Adder using MTCMOS Technology

The proposed one-bit MTCMOS full adder was designed with 18T (18 transistors). The functional block diagram and circuit diagram for the proposed full adder as shown in Figure 4.3 and Figure 4.4.

Because of the usage of a sleep transistor, the suggested full adder has lower mean power than a typical full adder. The primary goal of this study is to stimulate the suggested adder using the SPICE tool in four different technologies: 90nm, 70nm, 25nm, and 18nm.

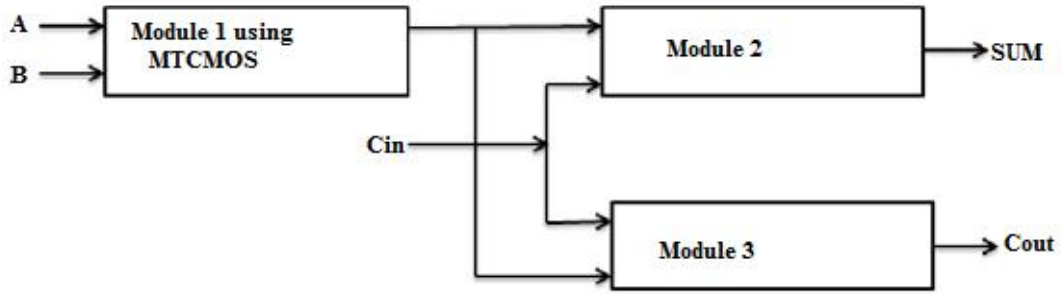


Figure 4.3 Block diagram of the proposed full adder

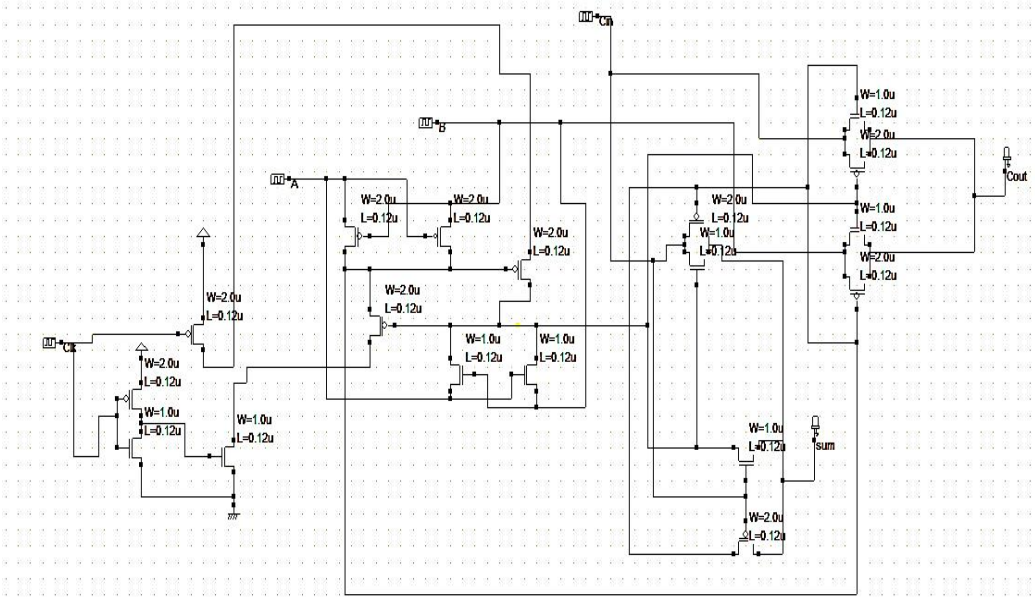


Figure 4.4 Circuit diagram of proposed full adder

Various nanoscale regimes are used in the design of the proposed complete adder, which results in a complex arrangement. In terms of space, power, and latency, a one-bit full adder implemented in MTCMOS technology was compared to a conventional approach. Figure 4.5 depicts the layout design for the proposed MTCMOS complete adder in 90nm technology, which is shown in red.

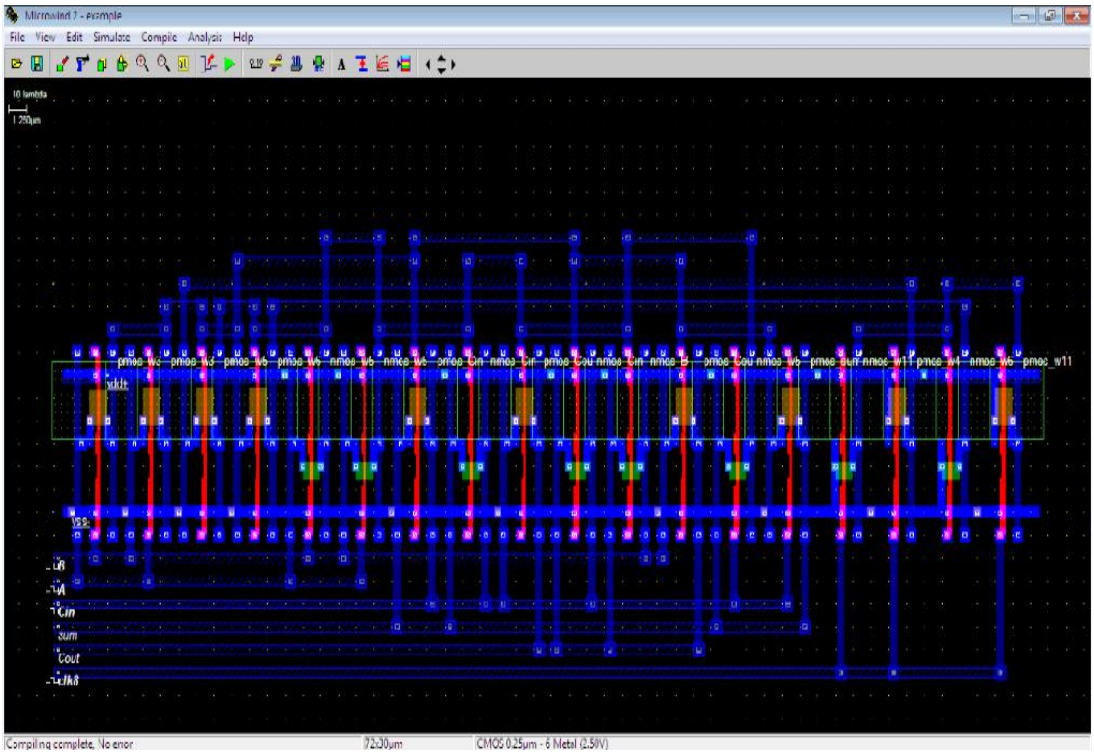


Figure 4.5 Layout diagram of the proposed full adder in 90nm technology

4.3.2 Proposed Array Multiplier using MTCMOS Technology in 90nm and 70nm Technology

The multiplier is one of the most important import blocks in the arithmetic logic unit. It performs a wide range of operations in signal processing applications, data manipulation applications, and image processing applications, among other things. It is shown here that the planned MTCMOS complete adder may be implemented in an array multiplier. The design that

was implemented in the SPICE tool is seen in Figure 4.6. The multiplier design was implemented in both 90nm and 70nm technologies, depending on the application. Analysis and comparison of the performance matrices for the proposed multiplier are carried out in several Nano scale regimes.

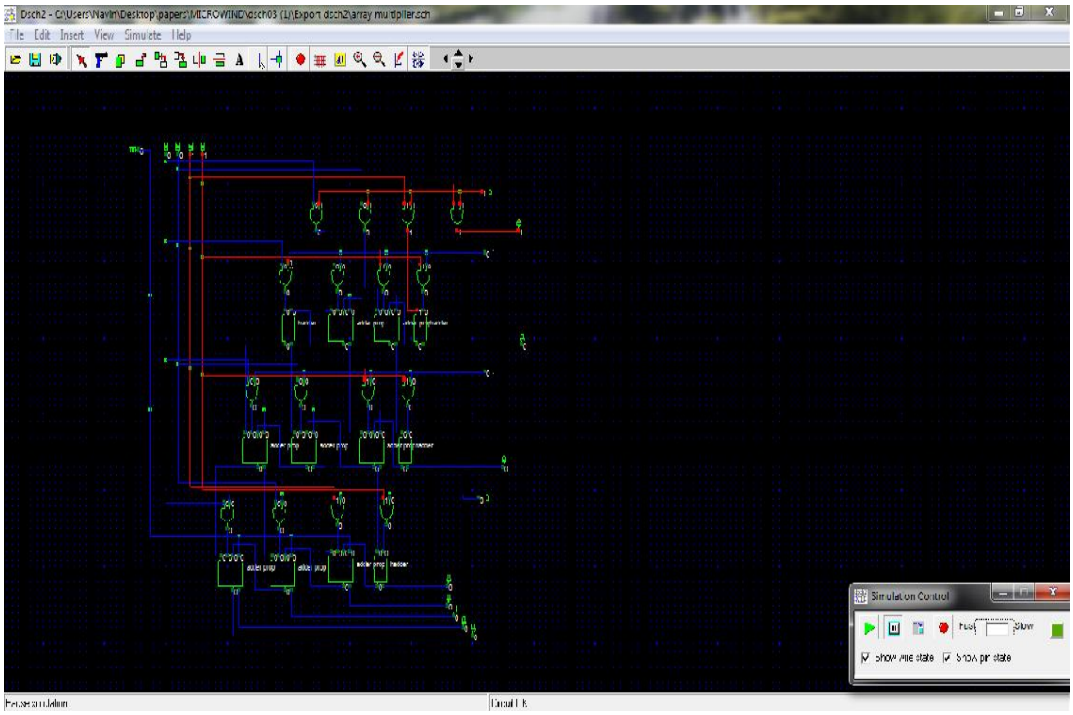


Figure 4.6 The array multiplier implementation using the proposed MTCMOS full adder

4.4 RESULT AND DISCUSSION

The SPICE tool was used to simulate the proposed MTCMOS one-bit full adder in four different technologies: 90nm, 70nm, 25nm, and 18nm. The suggested multiplier may be implemented in both 90nm and 70nm technologies, depending on the application. It is investigated in several nanoscale regimes how the transient behavior of an existing and suggested full adder and proposed multiplier changes over time. Figures 4.7, 4.8, 4.9, and 4.10 depict the transient reaction of the present and proposed adder and multiplier, respectively.

As shown in Table 4.1, the proposed adder's performance matrices (such as are, delay, and power) compare well with the present adder in different nanoscale regimes. Table 4.2 depicts a comparison of the performance of the present multiplier and the proposed multiplier in terms of area, power, and latency, respectively. The comparison charts in Figure 4.11 and 4.12 show the differences and similarities between the current and suggested adders for power and delay matrices, respectively.

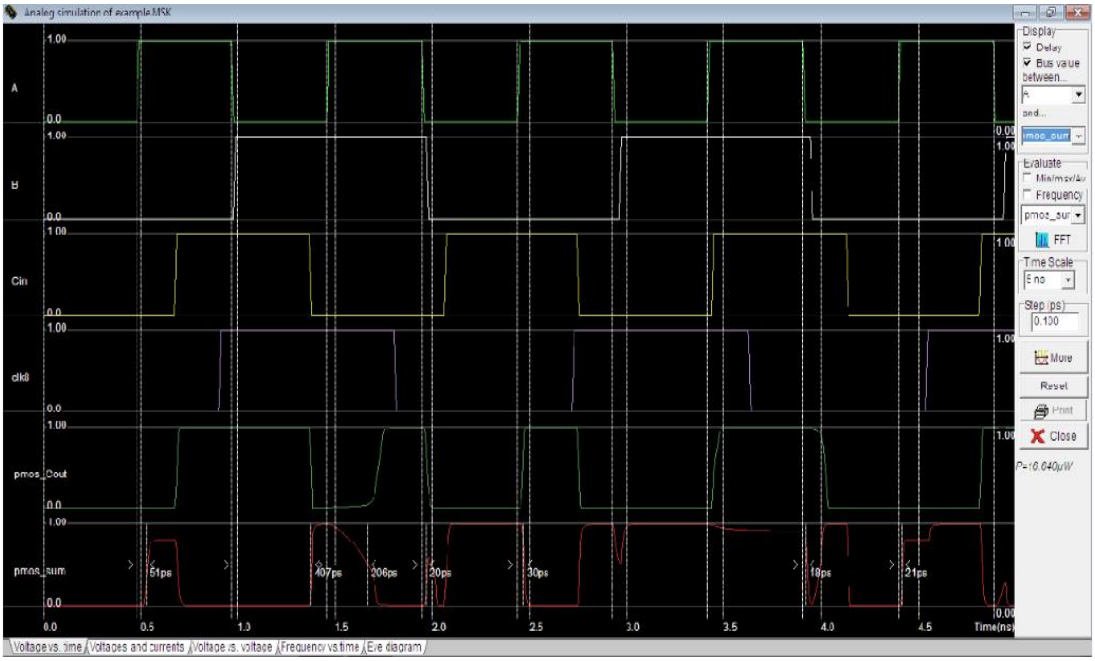


Figure 4.7 Transient analysis of the existing full adder

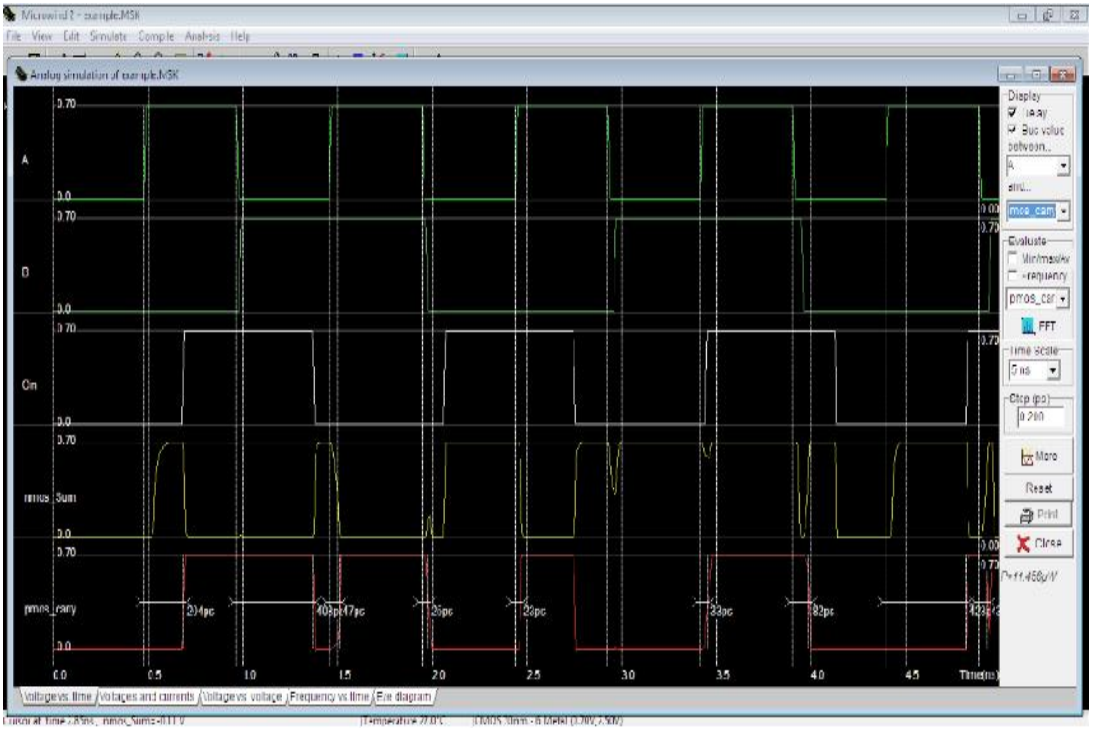


Figure 4.8 Transient analysis of the proposed full adder is 90nm

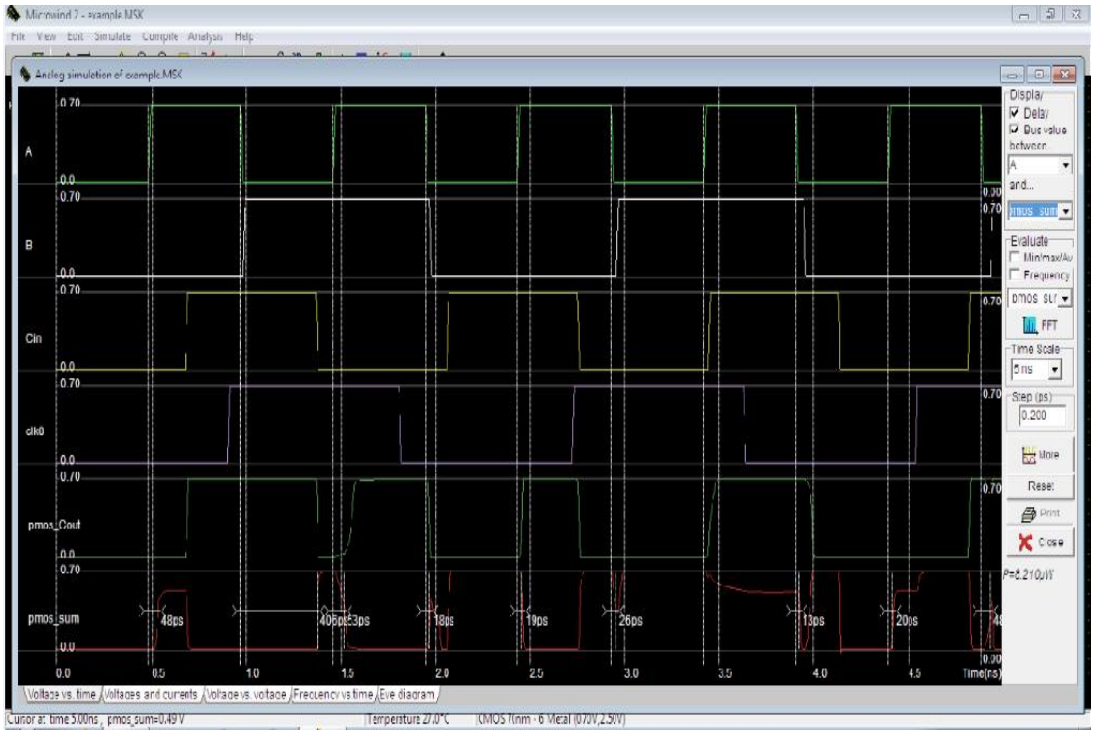


Figure 4.9 Transient Analysis of the proposed full adder is 70nm

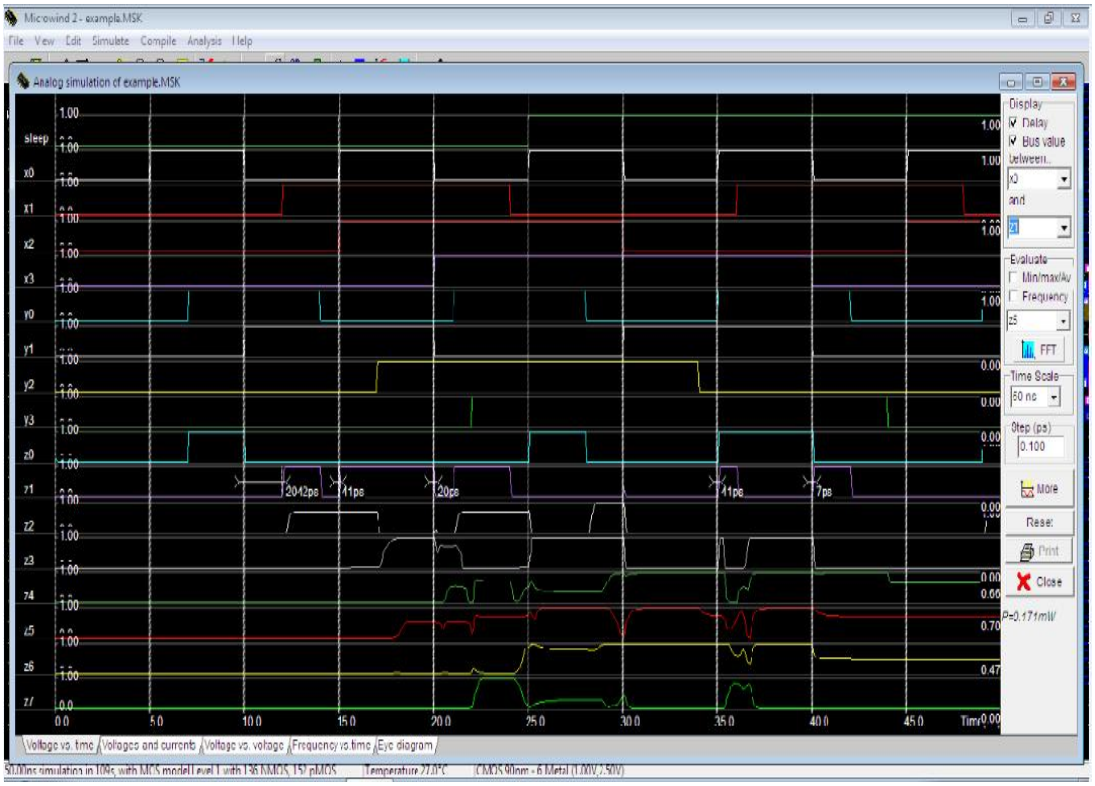


Figure 4.10 The simulation result for the proposed multiplier is 90nm

Table 4.1 Comparison of various matrices for the proposed full adder

Technology	**90nm**			**70nm**		
Metric	**Area (Sq.m)**	**Power (µW)**	**Delay (pS)**	**Area (Sq.m)**	**Power (µW)**	**Delay (pS)**
Existing	350	18.22	206	140	11.46	198
Proposed	517	16.64	190	297	8.21	170
Technology	**25 nm**			**18nm**		
Metric	**Area (Sq.m)**	**Power (µW)**	**Delay (pS)**	**Area (Sq.m)**	**Power (µW)**	**Delay (pS)**
Existing	96	7.78	150	66	3.57	112
Proposed	210	5.23	130	174	1.72	94

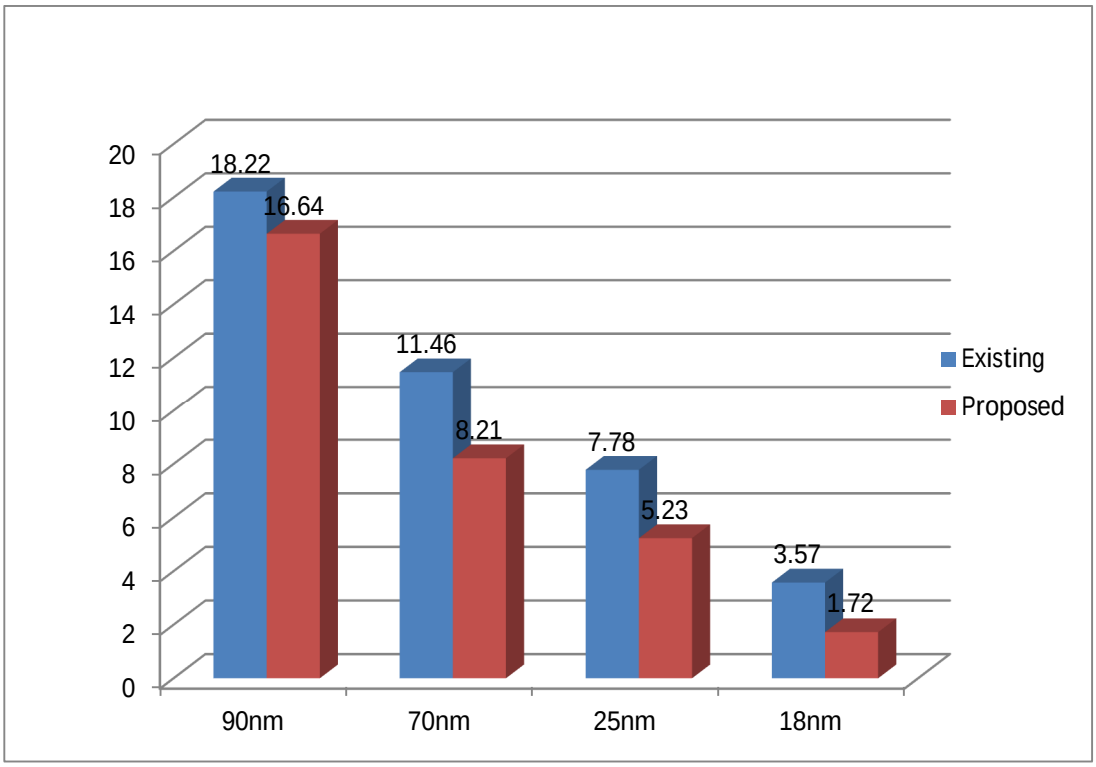


Figure 4.11 Comparison chart for power in the existing and proposed full adder

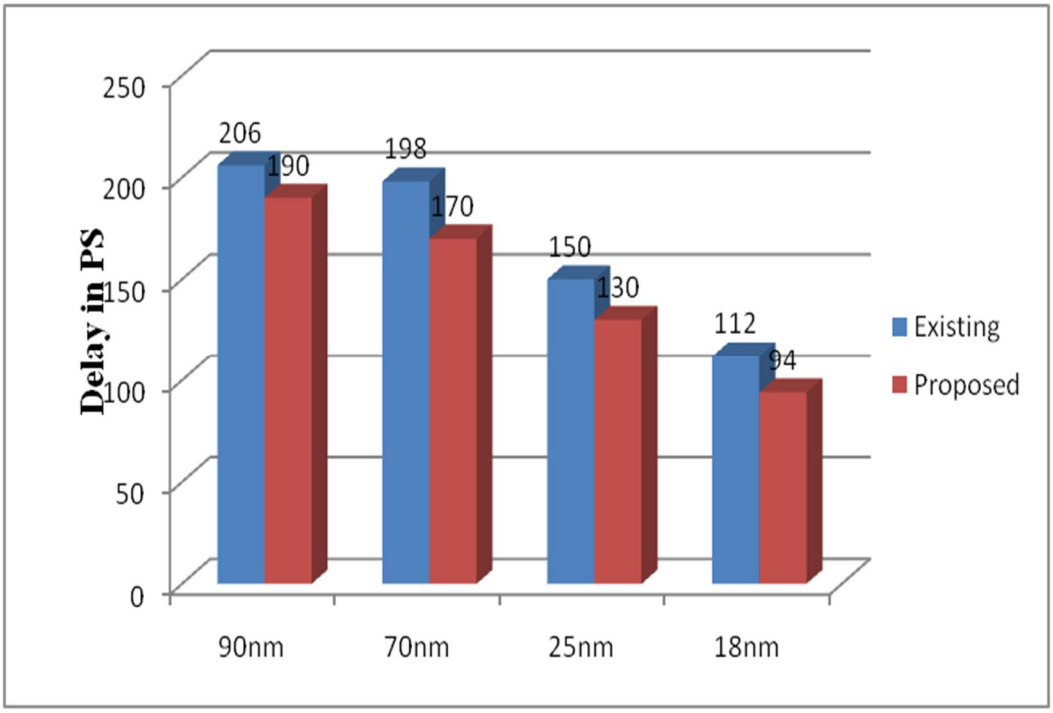


Figure 4.12 Comparison chart for the delay in existing and proposed full adder

Table 4.2 Comparison results of various matrices in existing and proposed Multiplier

Technology	90nm			70nm		
Metric	Area (Sq.m)	Power (µW)	Delay (pS)	Area (Sq.m)	Power (µW)	Delay (pS)
Existing	4294	69.244	46	3387	56.739	38
Proposed	5544	39.222	41	4472	36.722	34

4.5 SUMMARY

The 90nm, 70nm, 25nm, and 18nm technologies are used to implement the one-bit complete adder that was researched using the MTCMOS process. The traditional adder and the suggested adder were both developed and stimulated using the SPICE simulation program. It was also calculated and compared how different design parameters like area, power, and delay were. After comparing the power consumption of the one-bit full adder operating at 0.9v for 90nm and 70nm technologies, it was discovered that the overall power consumption for 90nm technology was 18.215 W, for 70nm technology was 11.46 W, for 25nm technology was 7.78 W, and for 18nm technology was 3.57 W. It is calculated that the proportion of delayed time minimized in the suggested full adder for 90nm is 190pS, for 70nm is 170pS, for 25nm is 130pS, and for 18nm is 94pS.

To maximize the total space utilization of the suggested adder, the number of transistors employed in the proposed design is raised. A similar approach was used in determining the power and delay of the proposed multiplier in the implementation section, which was determined to be 39.22W for 90nm technology and 36.722W for 70nm technology. Based on the comparison matrices, the suggested design reduces the overall power consumption as well as the delay when compared to the current design. As a result, this suggested design may be used for VLSI circuit applications that need low power and fast speed.

CHAPTER 5

A NOVEL DESIGN OF NANOSCALE TIEO-BASED SINGLE LAYER FULL ADDER AND FULL SUBTRACTOR IN THE QCA PARADIGM

5.1 SCOPE AND OBJECTIVE

One of the favorable technologies is a quantum dot cellular automaton (QCA) extremely low power at the nanoscale with high density and high-speed structures. Due to high energy usage and difficulty in further size reduction in CMOS technology is to reach flexible choices for the replacement of new technology. Among many technologies, CA is one of the budding technologies at the nanoscale.

This has delightful features such as lower energy consumption and less cell density in (Gargini 2000). The adder and subtractor are basic building blocks of arithmetic logic circuits. In this work, the efficient design of QCA full adder and full subtractor is proposed by using a novel three-input Exclusive OR (TIEO) gate. The designed circuits are stimulated with the QCA Designer tool and the power dissipation of the proposed designs has been estimated using the QCA Designer E tool.

5.2 RESEARCH METHODOLOGY

For the design of complex digital circuits, the exclusive OR (XOR) gate acts as a vital role. It can be used in many digital logic circuits such as adder and subtractor, some communication circuits such as parity generator and checker, and various blocks in the arithmetic logic units. QCA is one of the new technologies enabled for high performance with low power consumption.

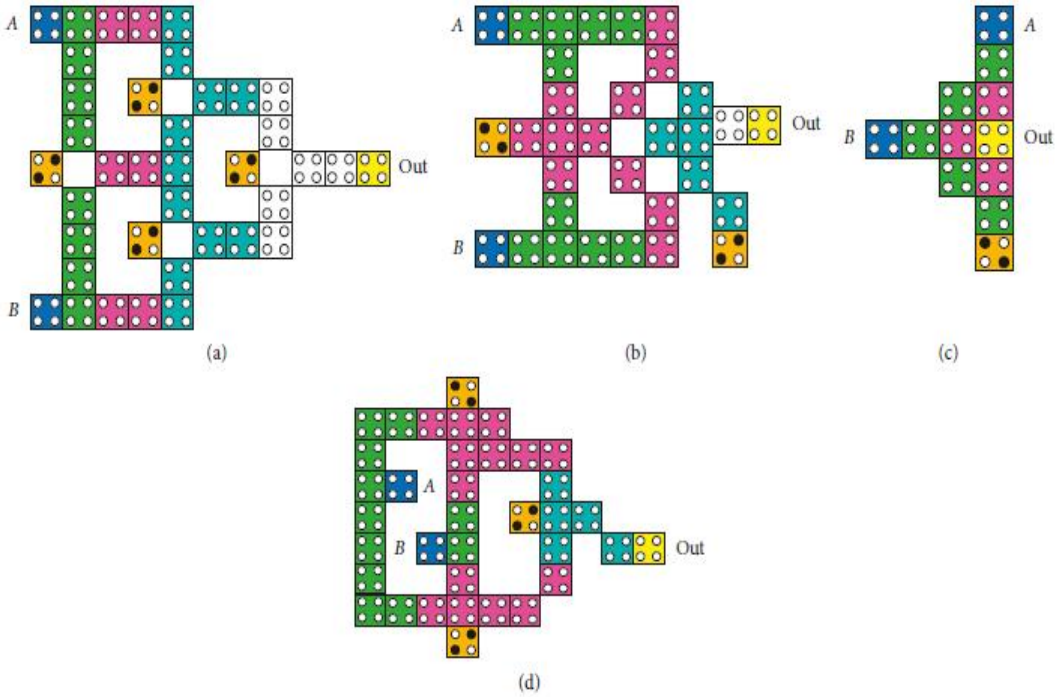


Figure 5.1 Previous Exclusive-OR gates (a) design in (Waje & Dakhole 2014) (b) design in (Poorhosseini & Hejazi 2018) (c) design in (Bahar *et al.* 2017) (d) design in (Singh *et al.* 2016)

In literature, various QCA layout structures for XOR gates were analyzed in (Berarzadeh *et al.* 2017, Singh *et al.* 2016, Waje & Dakhole 2014, Poorhosseini & Hejazi 2018, Bahar *et al.* 2017). The analyzed designs are a majority gate-based methodology. Generally XOR gate design with two inputs or three inputs in various layouts. In (Berarzadeh *et al.* 2017), the

authors have proposed a novel and robust XOR gate with 13 cells and a 0.012μm^2 area.

This design occupies less area than the other design. In (Singh *et al.* 2016), the authors have presented with 28cells and a 0.02 μm^2 area. In (Waje & Dakhole 2014), proposed with 36 cells, it occupies a 0.03 μm^2 area with a delay of 0.75 and it utilizes two majority gates and two inverter gates. The design was presented in (Poorhosseini & Hejazi, 2018) with 37 cells with the same area and delay as in (Waje & Dakhole 2014). The novel design of the XOR gate is achieved in (Bahar *et al.* 2017) with 12 cells, 0.02 μm^2 area with 1.25 delay. The previously designed EXOR gates are as shown in Figure 5.1.

5.3 PROPOSED WORK

5.3.1 Proposed QCA Three Input EXOR Gate

The new efficient three-input exclusive OR gate is proposed with 8 cells. The proposed design occupies a 0.01 μm^2 area and 0.5 delays. Without the use of the majority gate to achieve the proposed three input EXOR gate design. The designed circuit functionality is verified using the QCA designer tool. The proposed QCA design and its symbol suggested and proposed structures are shown in Figure 5.2.

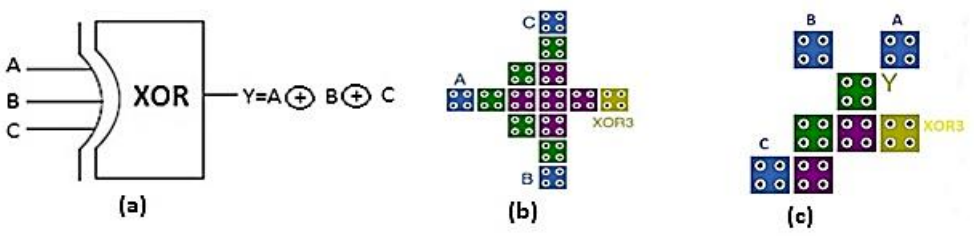


Figure 5.2 Three Input XOR Gate (a) Symbol (b) Suggested QCA Layout (c) Proposed QCA layout

5.3.2 Proposed One-Bit Full Adder using Three Input EXOR Gate

From the literature, various QCA design for one-bit full adder is observed. In these designs, the majority of gate designs are utilized. Generally, a one-bit full adder has two outputs sum and carry and three inputs A, B, Cin. Equation 4.1 and 4.2 tells the simplified expression for the outputs of one-bit full adder

Sum=ABCin+A'B'Cin+A'BCin'+AB'Cin' (4.1)

$$Cout = AB + BCin + ACin \quad (4.2)$$

The various minimized structures of the full adder are reviewed in (Rumi *et al.* 2014, Azghadi *et al.* 2007, Cho & Swartzlander 2009, Mohammadi *et al.* 2016). These structures are minimized by the reduction and rearrangements of the majority gate.

The previous minimized structures are shown in Figure 5.3. The minimized equations for the minimized structures of the reviewed design are intimated in equations 4.3 to 4.7. These expressions denote the output sum expression for the one-bit adder. For carrying output, a single majority gate is enough for the design.

In our references, the various minimized structures of a one-bit full adder can be reviewed in terms of the majority gate. Based on the minimized structures the equation of sum is expressed as follows.

$$Sum = Maj(Maj(A, B', Cin), Maj(A, B, Cin'), Maj(A', B, Cin) \quad (4.3)$$

$$Sum = Maj(Maj(A', B, Cin), Maj(A, B', Cin), Cin') \quad (4.4)$$

$$Sum = Maj(Maj(A, B, Cin'), Cout', Cin)) \quad (4.5)$$

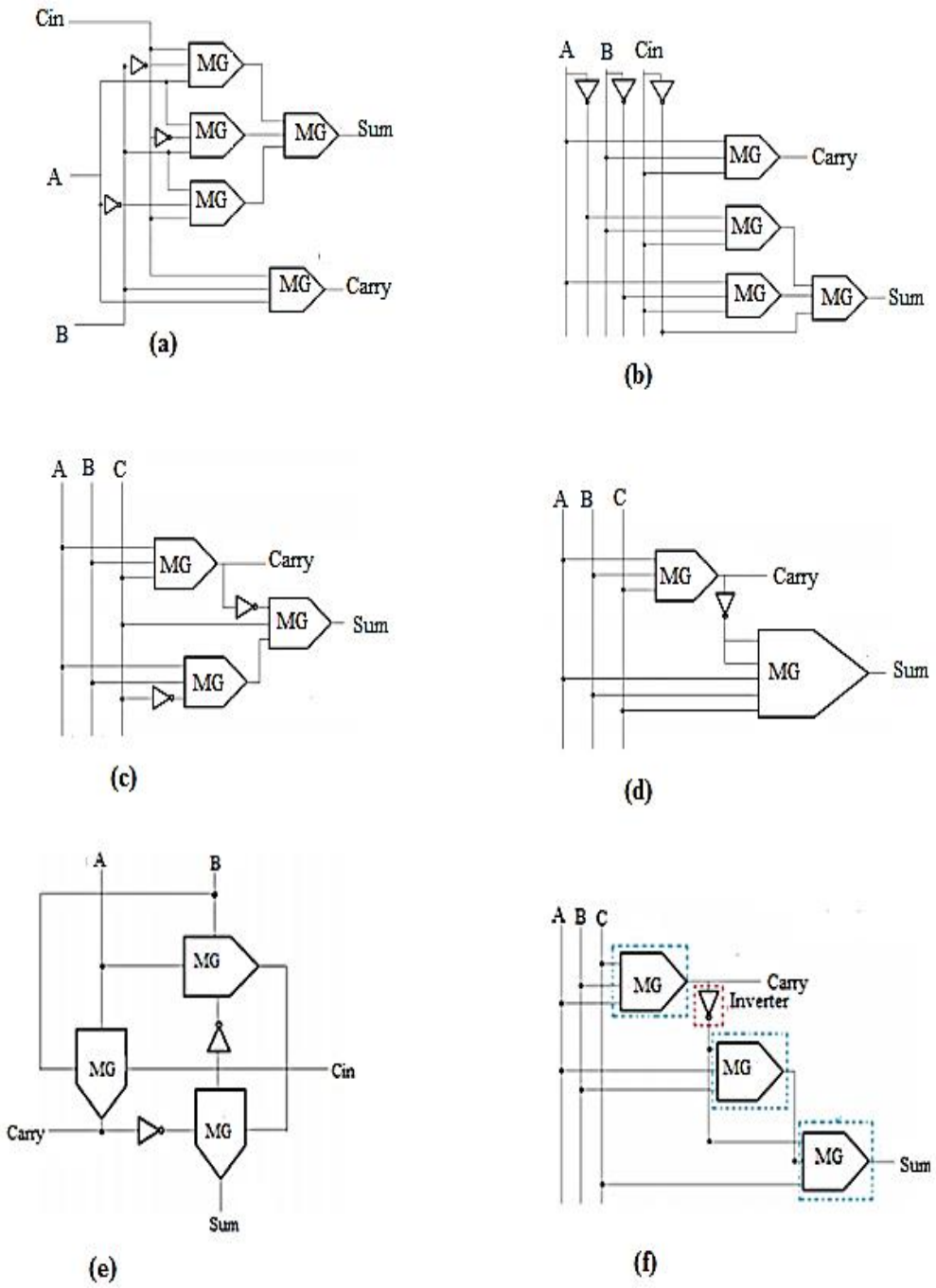


Figure 5.3 The previous design of one bit full adder (a) design in (Pougaw & Lent 1994) (b) design in (Navi *et al.* 2010) (c) design in (Rumi *et al.* 2004) (d) design in (Azghadi *et al.* 2007) (d) design in [43] (e) design in (Mohammadi *et al.* 2016)

$$Sum = Maj5(A, B, Cin, Cout', Cout) \tag{4.6}$$

$$Sum = Maj\big(Cout', Cin, Maj(A, B, Cin')\big) \tag{4.7}$$

Figure 5.4 (a) shows the schematic and QCA layout structure for a one-bit full adder based on three inputs EXOR gate using five input majority gate presented in (Angizi *et al.* 2015).

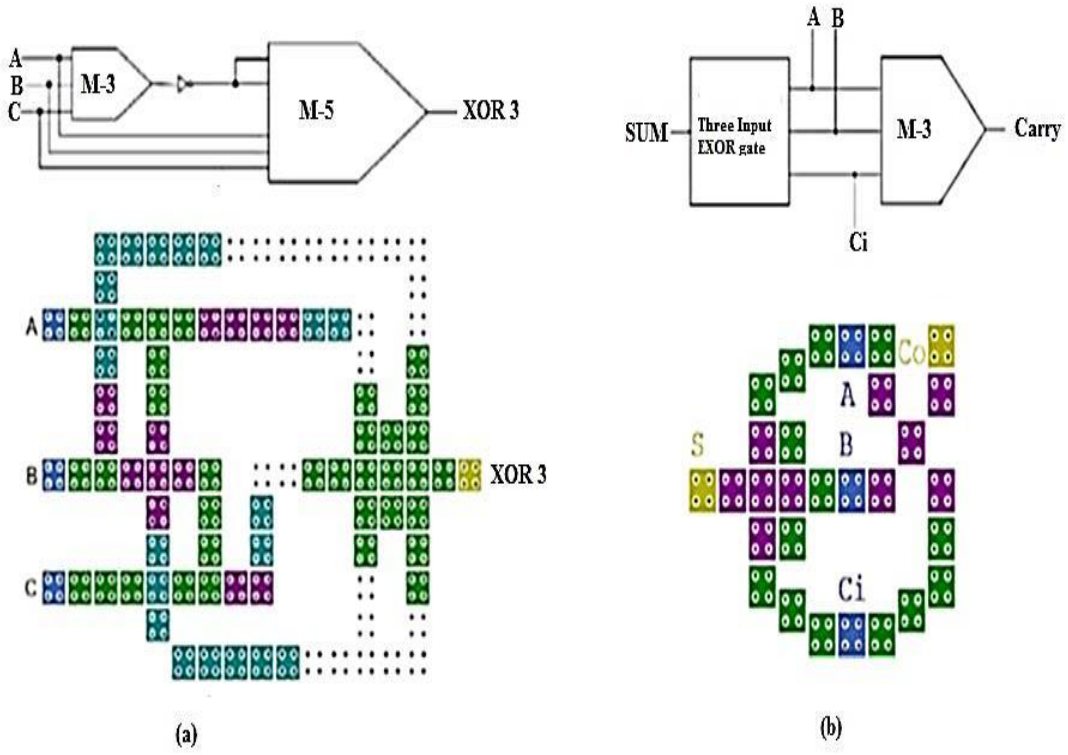
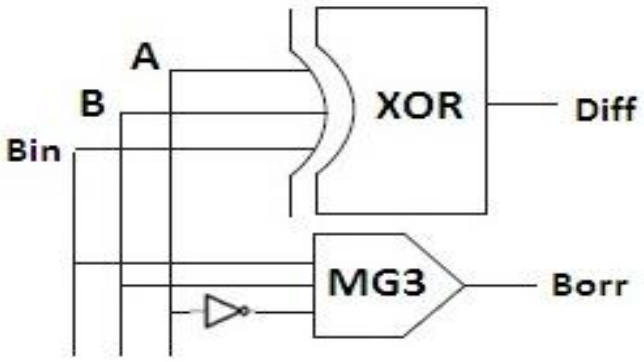


Figure 5.4 The previous design of TIEO gate (a) design of three input XOR gates in (Angizi *et al.* 2015) (b) design one-bit full adder using TIEO in (Balali *et al.* 2017)

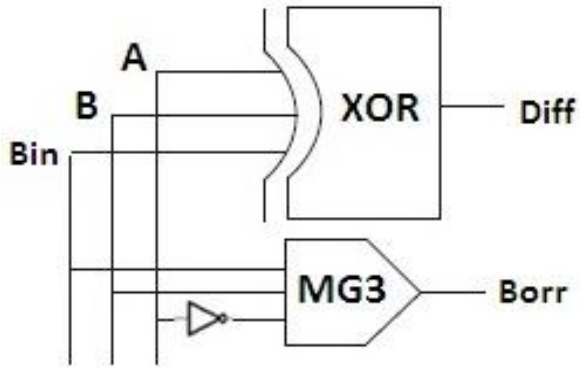
Figure 5.4 (b) shows the schematic and QCA layout structure for a one-bit full adder based on three inputs EXOR gate using a three-input majority gate presented in Moslem Balali, (2017) with the utilization of 14 cells for EXOR gate and 29 cells for the full adder.

In this work, the design of a one-bit full adder is proposed in three ways (i) Three input EXOR gate with 14 cells for sum operation and Cout operation carried out by normal three-input majority gate with 45cells (ii) Using TIEO and rotated majority gate with 31 cells with input A, B, Cin

as shown in Figure 5.6 (a) and Figure 5.6(b). (iii) Figure 5.6 (c) shows the QCA layout for the one-bit full adder using the proposed TIEO with 21 cells. Comparative to other designs the proposed structure has less number of cells. Figure 5.5 shows the schematic structure for the proposed designs.



(a)



(b)

Figure 5.5 Full adder logical diagram using TIEO gate (a) The proposed one-bit full adder (b) The proposed one-bit full subtractor

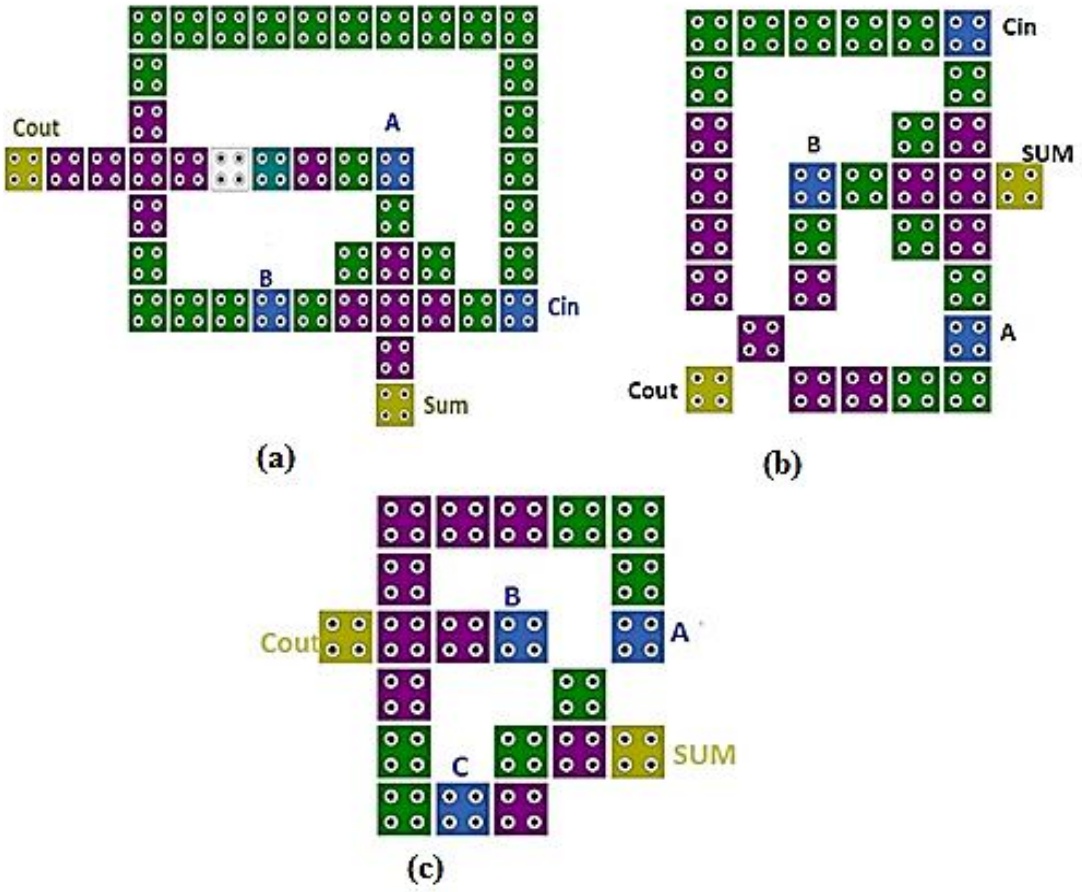


Figure 5.6 Three proposed full adder QCA layouts with proposed TIEO gate

5.3.3 Proposed One Bit Full Subtractor using Three Input EXOR Gate

The proposed one-bit full subtractor circuit is designed with three input EXOR gates with the output expressions of equations (4-8) & (4-9).

$$Difference = A \text{ ^} B \text{^} Bin \tag{4.8}$$

$$Bout = A'B + BBin + A'Bin \tag{4.9}$$

The three different designs of the proposed one-bit full adder QCA layouts are shown in Figures 5.7. Design 1 utilizes 44 cells and design 2

utilizes 30 cells and design 3 utilizes 20 cells. Comparative to other designs, the proposed design to achieve the correct operation with less number of cells.

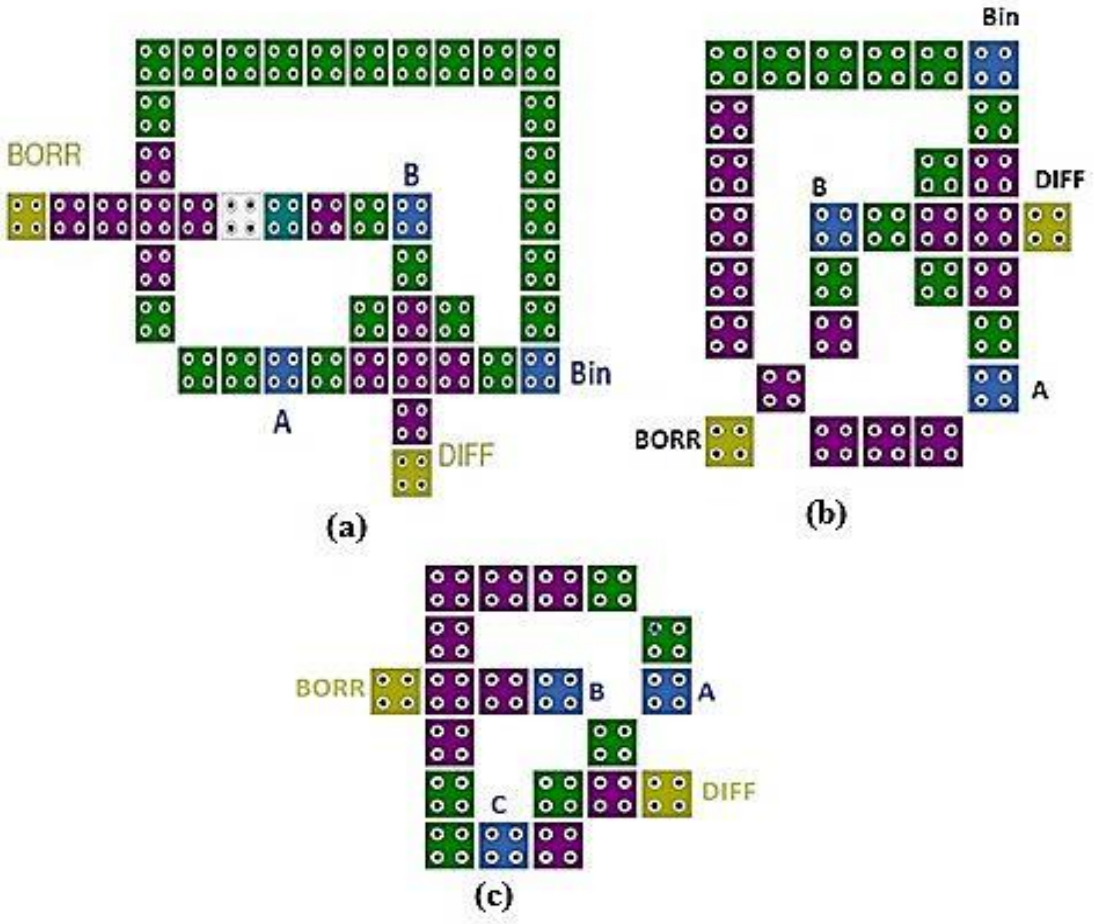


Figure 5.7 Three proposed full subtractor QCA Layout with proposed TIEO gate

5.4 POWER ANALYSIS

The QCADesigner-E tool has one more special simulation engine available for the calculation of Energy dissipation in eV, name as Coherence vector energy engine (w/Energy). This tool is helping in calculating the energy dissipation for QCA circuits. In this work, the energy dissipation for the proposed circuit is analyzed by using the QCADesigner-E tool.

This tool helps in the calculation of energy dissipation for the QCA circuit as shown in Table 5.1 and Table 5.2 for the proposed full adder and full subractor. This tool includes three different simulation engine setups that are, the coherence vector, the coherence vector (w/energy), and bistable approximation.

Table 5.1 Proposed Full Adder Power Dissipation

E_ bath_ total (E_{btx}) (meV)	**E_clk_total (Ex) (meV)**	**E_Error_ Total (E_{Etx}) (meV)**	**Sum_bath (S_b)**	**Avg_bath (A_b)**
2.4010	2.0478	-0.23139	3.11 e-002 eV (Er:-3.11 e-003 eV)	2.83 e-003 eV (Er:-2.83 e-004 eV)
2.7444	0.94057	-0.26084		
2.9822	0.33593	-0.31536		
3.3834	0.81947	-0.34484		
2.9861	0.81557	-0.29866		
3.1385	0.32446	-0.31646		
2.5664	9.3612	-0.24068		
2.7753	2.0628	-0.29366		
2.4010	2.0478	-0.23139		
2.7444	0.9405	-0.26084		
2.9822	0.3359	-0.31536		

Table 5.2 Proposed Full Subtractor Power Dissipation

E_ bath_ total (E_{btx})(meV)	E_clk_total (E_{ctx})(meV)	E_Error_total (E_{Etx})(meV)	Diff_bath (D_b)	Avg_bath (A_b)
2.0379	1.3907	-0.20469	2.65 e-002 eV (Er: -2.70 e-003 eV)	2.41 e-003 eV (Er: -2.45 e-004 eV)
2.1155	0.72042	-0.21211		
2.8734	0.17893	-0.29609		
2.6156	0.52103	-0.26924		
2.2488	0.52104	-0.22982		
3.0913	0.17894	-0.32179		
1.9821	0.72041	-0.19676		
2.4823	1.3907	-0.25339		
2.0379	1.3907	-0.20469		
2.1155	0.72042	-0.21211		
2.8734	0.17893	-0.29609		

5.5 RESULT AND DISCUSSION

The suggested plan of three input EXOR gates, one-bit full adder, and one-bit full subtractor stimulated and verified the functionality using the QCA Designer tool. The simulation results of the proposed designs show in Figure 5.8, Figure 5.9 and Figure 5.10.

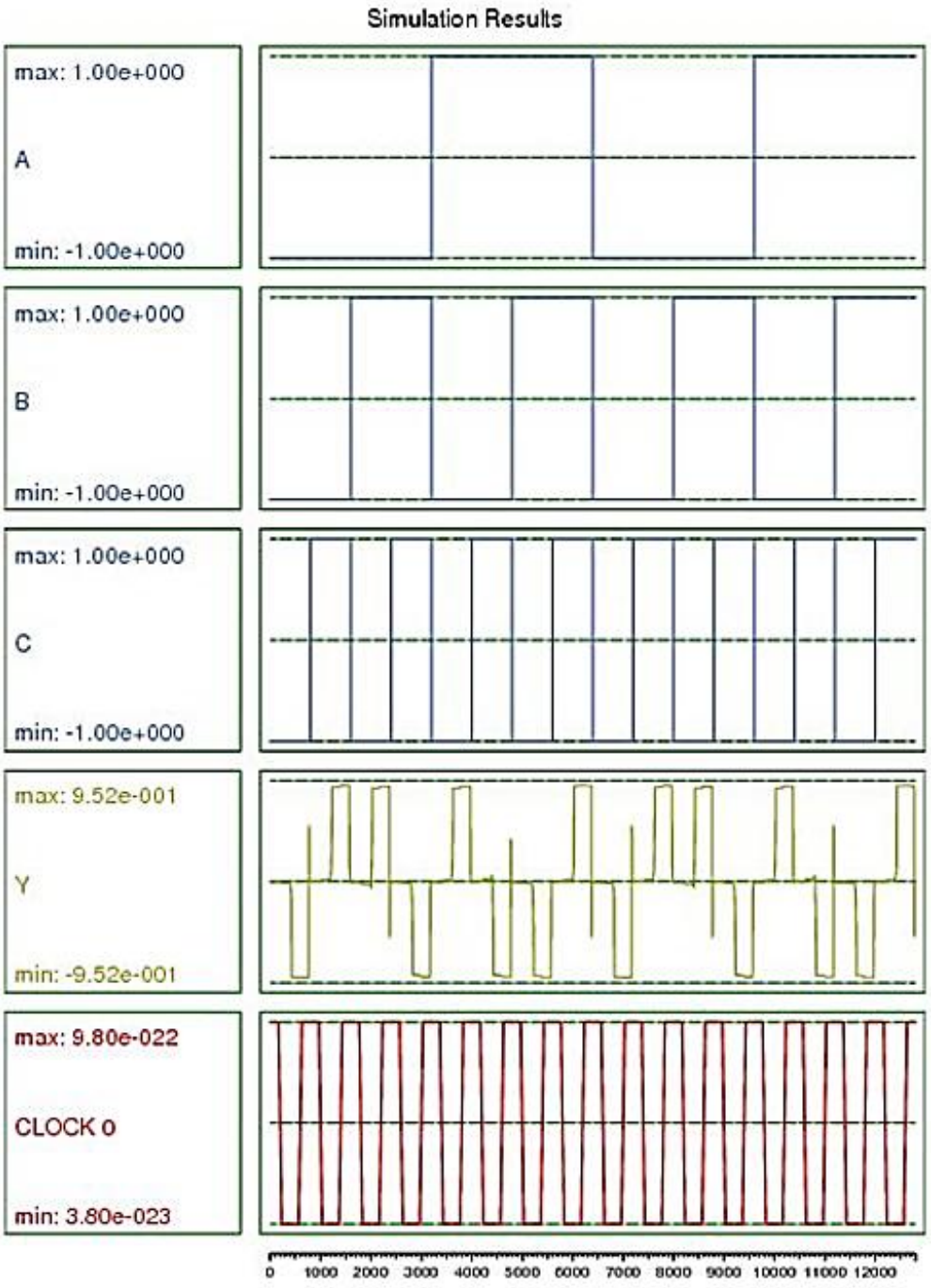


Figure 5.8 Simulation result for the planned three input EXOR gate

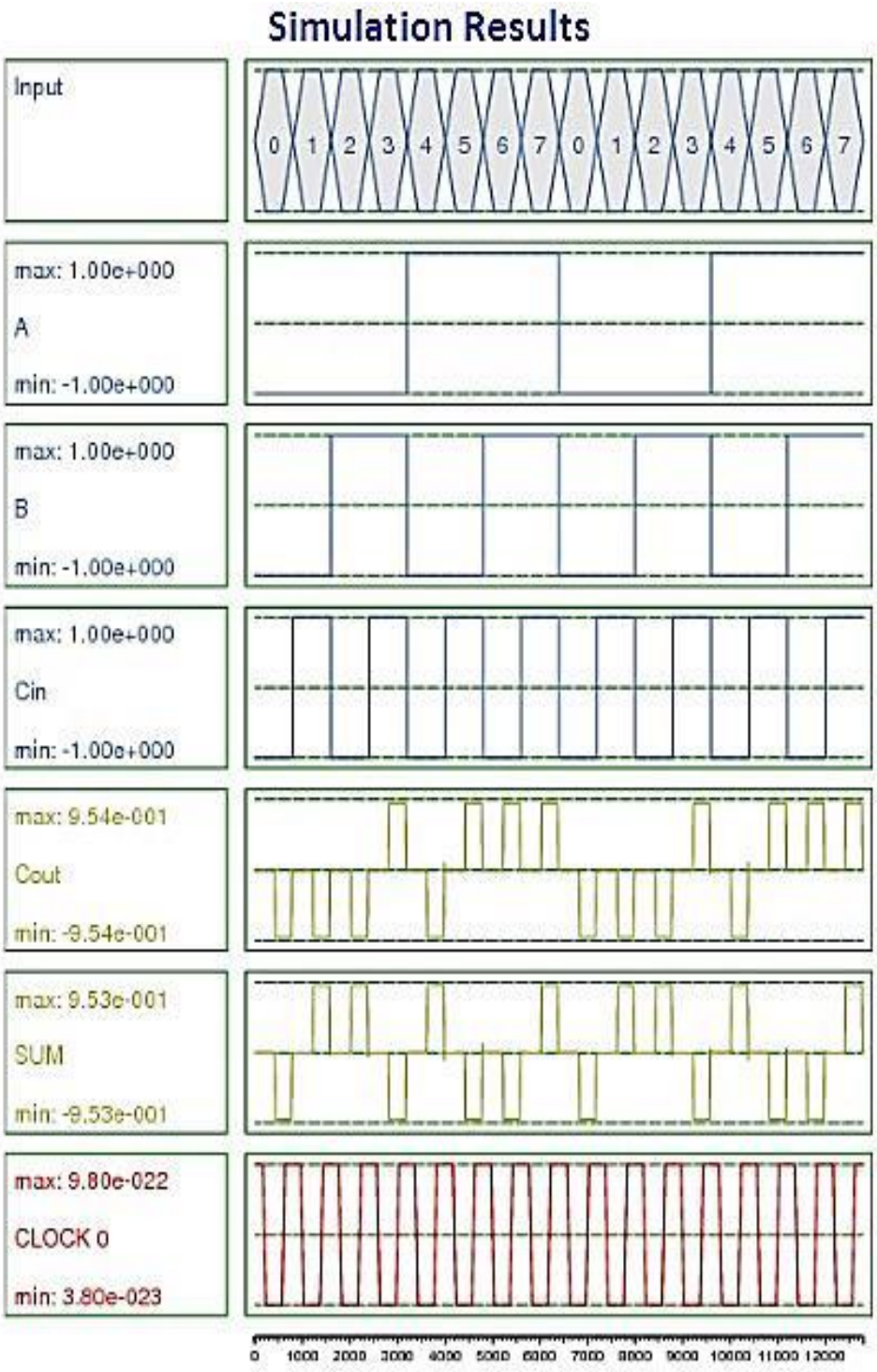


Figure 5.9 Simulation result for the planned full adder

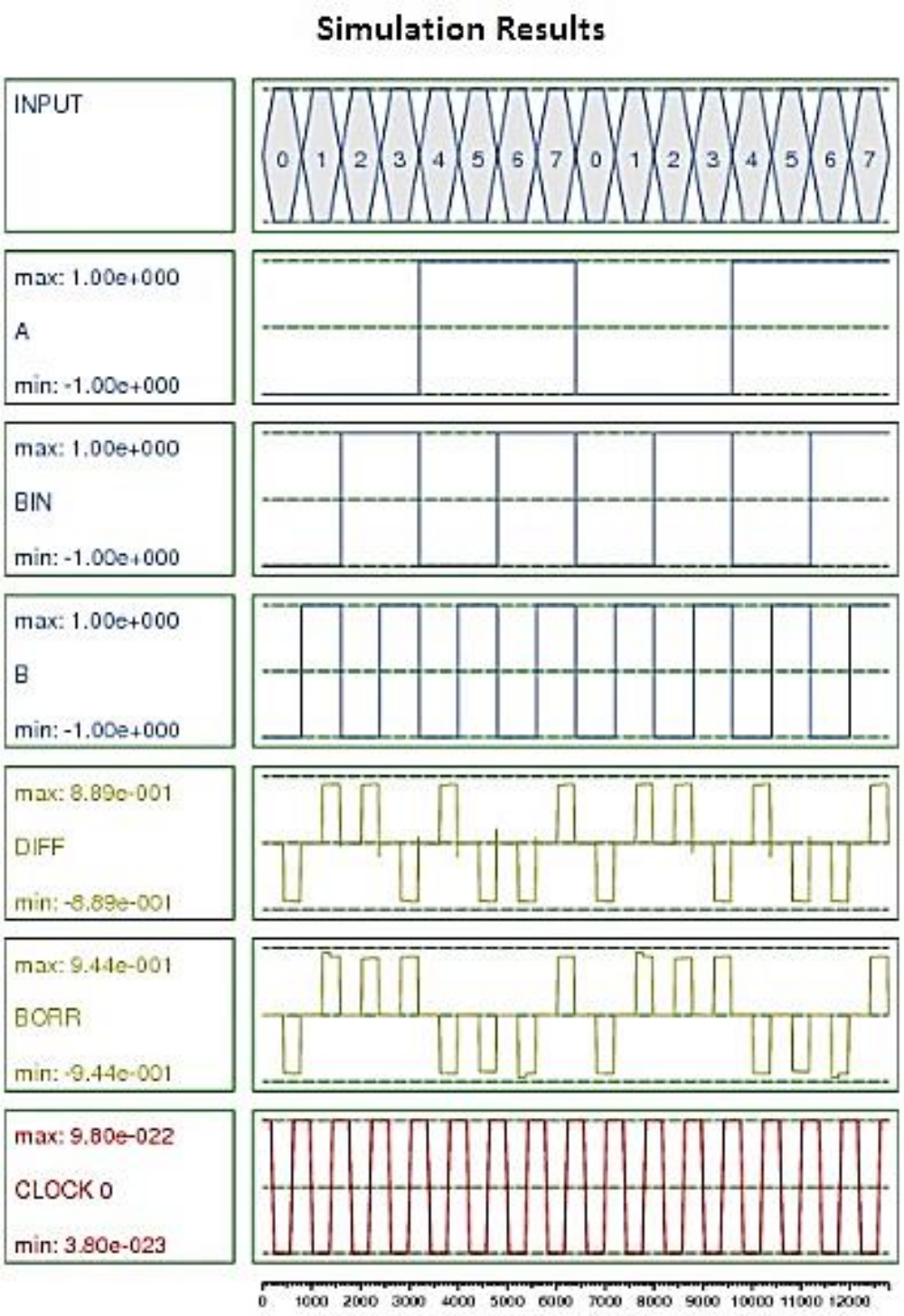


Figure 5.10 Simulation result for the planned full subtractor

The performance matrices like several cells utilized, area, latency, and cross-over type for three input EXOR gates are listed in Table 5.3. The performance matrices for the proposed full adder and full subtractor using majority gate-based and TIEO based designs are listed in Table 5.4.

Table 5.3 Comparison of the proposed three-input exclusive-OR gate with the existing designs

Reference	Cell count	Area (μm2)	Clock no.cycle	Crossover type
XOR(Niemier, 2000)	60	0.09	1.5	Coplanar
XOR (Hashemi *et al.* 2013)	54	0.08	1.5	Coplanar
XOR (Angizi *et al.* 2014)	67	0.06	1.25	Coplanar
XOR (Poorhosseini & Hejazi 2018)	37	0.03	1	Not Required
XOR (Waje & Dakhole 2014)	36	0.03	0.75	Not Required
XOR (Singh *et al.* 2016)	28	0.02	0.75	Not Required
XOR (Berarzadeh *et al.* 2017)	13	0.012	0.5	Not Required
XOR (Balali *et al.* 2017)	12	0.011	0.5	Not Required
Proposed three-input exclusive-OR gate (TIEO)	8	0.01	0.25	Not Required

Table 5.4 Comparison of the proposed one-bit full adder and full subtractor with the existing designs

Reference	Cell count	Type	Area (μm^2)	Clock No. cycle	Crossover type
(Pougaw, & Lent 1994)	192	Majority Gate	0.20	Not applicable	Multilayer
(Rumi *et al.* 2004)	145	Majority Gate	0.17	5	Multilayer
(Cho & Swartzlander, 2009)	86	Majority Gate	0.10	3	Coplanar
(Navi *et al.* 2009)	73	Majority Gate	0.04	3	Coplanar
Azghadi *et al.* 2007	51	Majority Gate	0.03	3	Coplanar
(Mohammadi *et al.* 2016)	38	Majority Gate	0.02	3	Multilayer
(Angizi *et al.* 2014)	94	TIEO	0.02	2	Not required
(Balali *et al.* 2017)	29	TIEO	0.02	2	Not required
Proposed Full adder					
Design1	45	TIEO	0.02	2	Not required
Design2	31	TIEO	0.02	2	Not required
Design3	21	TIEO	0.02	1.5	Not required
Proposed Full Subtractor					
Design1	44	TIEO	0.02	2	Not required
Design2	30	TIEO	0.02	2	Not required
Design3	20	TIEO	0.02	1.5	Not required

5.6 SUMMARY

In this work presented an efficient nanostructure for TIEO with 8 cells. In the implementation part, the one-bit full adder and one-bit full subtractor are presented. The performance matrices for existing and proposed are compared and analyzed in Table 5.3 and Table 5.4. The proposed QCA logic circuits are simulated based on a bistable approximation simulation engine with the features of radius 65nm, relative permittivity: 12.90, clock high level: 9.8e-22J, clock low-level: 3.8e-23J, separation of layer:11.50 nm, overall simulation period:7.0e-011s, and samples number:12800. In our suggested plan, to get high performance with less count by the use three-input XOR gate design with a single layer. The suggested adder and subtractor perform reliably well. Its clocking phase is realized fast. In suggested full adder plan uses 44 cells to design1and 31cells in desgin2 with two clock phases and a 0.02 μm^2 area approximately as shown in Fig 12. Similar way the proposed design of the full subtractor uses 43cells in design1 and 30 cells in design2 with two clock phases and a 0.02 μm^2 area approximately. Also average power dissipation of full adder is 2.83e-003 eV with Error voltage 2.83e-004 eV and average power dissipation for full subtractor 2.41e-003 eV with Error voltage -2.45e-004 eV can be obtained with QCADesigner E tool.

CHAPTER 6

AN EFFICIENT NANOSCALE SEQUENTIAL CIRCUIT WITH CLOCK INHERENT CAPABILITY IN QCA FOR FAST COMPUTATION PARADIGM

6.1 SCOPE AND OBJECTIVE

In the designing field, sequential circuits play a vital role compared to conventional circuit design. Hence the design of the sequential circuit meets the complexity. The complexity of circuit design is reliably reduced by the use of quantum-dot cellular automata.

One of the new and smart methods is quantum-dot cellular automata (QCA). It is useful for designing and implementing digital circuits with high performance and low power consumption at the nanoscale. It is transistor-less technology and this technology gives less power dissipation than CMOS technology.

The binary information in CMOS technology is represented in terms of current and voltages. In QCA the binary information is represented by the position of electrons within the quantum dot (Porod 1997, Orlov *et al.* 1999). This work presents a novel design of pulse generator, D flip-flop, and asynchronous counter by frequency divider methodology.

6.2 RESEARCH METHODOLOGY

Different studies in sequential circuit design and its QCA structures have been studied for reference. Sequential circuit design in QCA is significantly different from the conventional designs in CMOS technology. Hence it is more attractive attention in research. The sequential circuit designs are inherently pipelined and need a clocking scheme. One of the attractive areas in sequential design is memory and flip-flop design. Flip-flops are acting a major role in the design of sequential logic with supplementary combinational logic circuits. In (Navi 2010, Angizi *et al.* 2015) various structures of memory design and flip-flop design in QCA have been introduced.

The QCA flip-flop designs are line-based, loop-based, and majority gate-based structural designs. Based on design complexity in flip-flop, the design come under the category of loop-based, a line-based (or) majority gate-based structure. In (Berzon *et al.* 1999, Vankamamidi *et al.* 2008) line based structures are presented. The loop-based structures are presented in (Vankamamidi et *al.* 2005, Taskin et *al.* 2008).In (Vetteth *et al.* 2003) loop oriented QCA structures with coplanar crossover are presented. Some line-based designs without crossover techniques are presented in (Sara Hashemi & Keivan Navi 2012, Sabbaghi-Nadooshan & Kianpour 2014).

A majority gate-based design of D flip-flop is presented with less number of cells in Rezaei (2018), Abutaleb (2017). Flip-flop-based multiplexer design is presented in (Sabbaghi & Kianpour 2014, Goswami *et al.* 2014). A majority of the gate-based design of the D flipflop is presented in (Rezaei 2018, Abutaleb 2017). A line-based previous structure of the D flip-flop is presented in Figure 6.1 (a) and Figure 6.1(b) and a loop-

based structure implemented in the design of the counter is presented in Figure 6.1(c). The majority of the gate-based design of the D flip-flop is presented in Figure 6.1(d) and Figure 6.1(e).

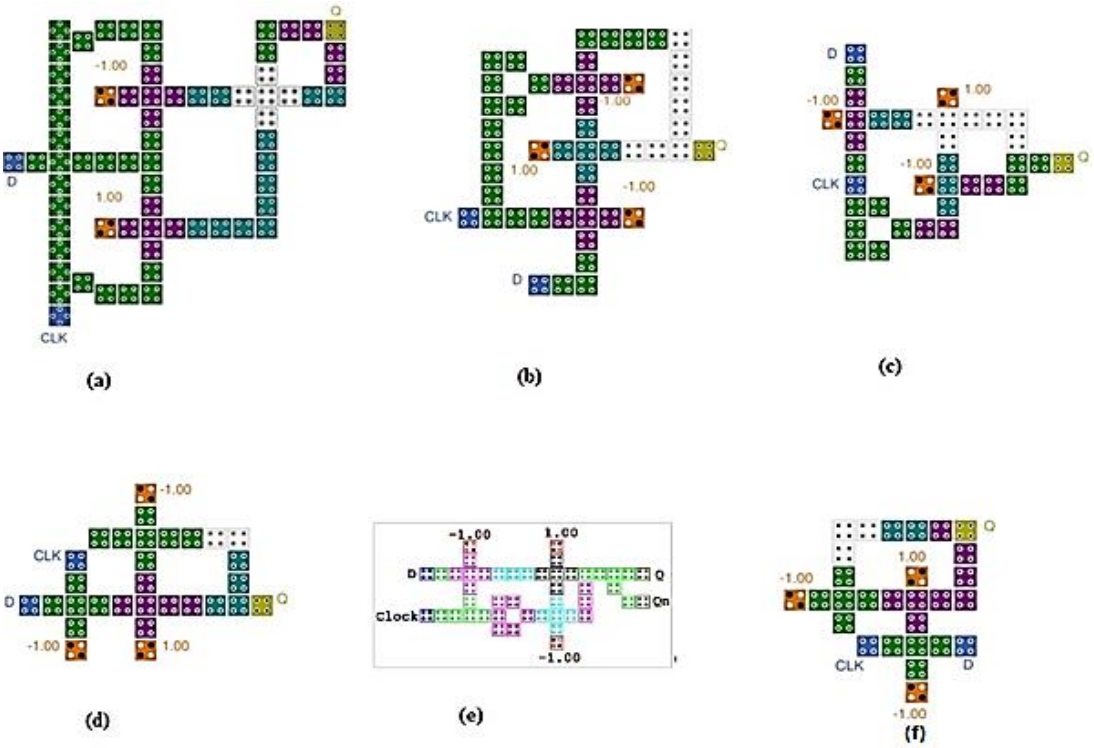


Figure 6.1 Various structures of D flip-flop (a) design in (Vetteth *et al.* 2003) (b) design in (Hashemi & Navi 2012) (c) design in (Sabbaghi & Kianpour 2014) (d) design in (Goswami *et al.* 2014) (e) design in (Rezaei 2018) (f) design in (Abutaleb 2017)

This research work suggested an efficient design of a majority gate-based D flip-flop with a pulse generator is presented.

6.3 PROPOSED WORK

6.3.1 Proposed Pulse Generator

For sequential circuit design, the clock signal plays a vital role. The output of the sequential circuits is controlled by the clock signal. That is it determines when and how the memory elements change their outputs. If a

sequential circuit is not having any clock signal as input, the output of the circuit will change randomly. It is mainly used for the synchronization of the circuit operation. For some circuit operation pulses are used instead of clock signals. With the help of some external circuits, the clock signals are converted into pulses. In this research work, the pulse generator helps to generate pulses and it helps to trigger the counter. The output pulse is generated when the input is assigned by IN=1 & CN=0.For the remaining combination IN=0 & CN=0, IN=0 & CN=1 and IN=1 & CN=1 the output of pulse generator is zero. Figure 6.2 (a) and Figure 6.2 (b) shows the gate-based and majority of the gate-based design of pulse generator with input IN, CN, and output. Figure 6.2(c) shows the QCA layout for the proposed pulse generator. The logical functions of the pulse generator are expressed in equation 6.1.

$$Output\ Y = Maj(IN, 0, (Maj(IN, CN, 0)') \tag{6.1}$$

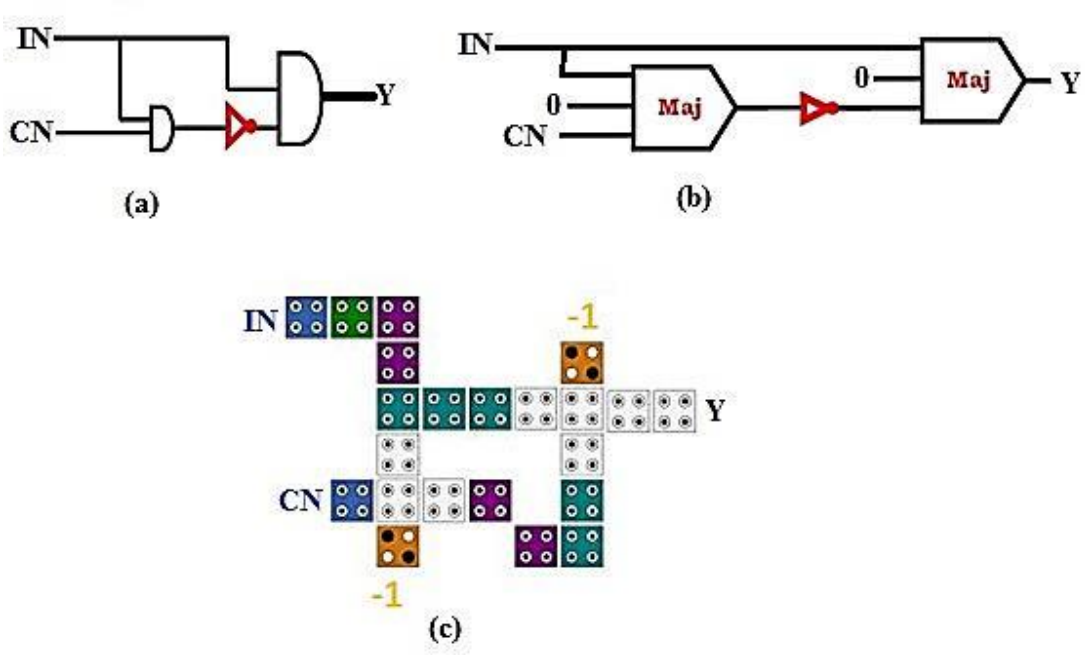


Figure 6.2 Proposed pulse generator (a) Gate based design (b) Majority gate based design (c) Layout for the proposed design

6.3.2 Proposed Design of D Flip-Flop

Flip-flop is the basic storage element in sequential logic. It acts as one main building block of digital circuits which are used in the computer, communications, and many other types of systems. Among various types, the D flip-flop is the most important because it captures the value of input data at a definite portion of the clock. At other times, the output Q does not change. So D flip-flop is widely used in circuit design. It is also known as a “data” (or) “delay” flip-flop. This flip-flop can be viewed as a memory cell.

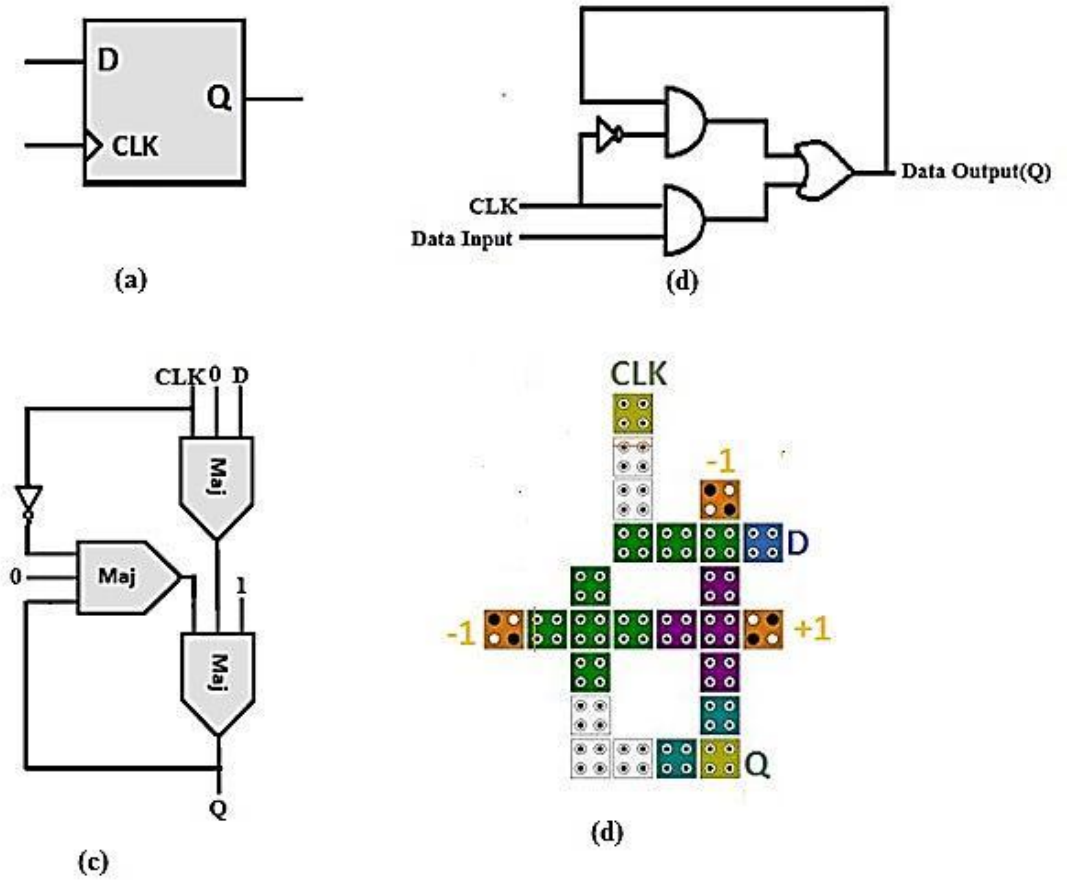


Figure 6.3 Proposed design of D flip-flop (a) Symbol (b) Gate based design (b) Majority gate based design (c) Layout for the proposed design

Here a new innovative D flip-flop QCA design is introduced to implement different sequential circuits in QCA technology, especially the QCA counter in this work. Figures 6.3 (a), 6.3 (b), and 6.3 (c) shows the graphic symbol, gate-based, and majority of gate-based circuits. Figure 6.3(d) shows the QCA layout for the proposed circuit design.

Equations 6.2 and 6.3 give the logical expressions of D flip-flop in terms of majority gate. Table 6.1 shows the various state operation of the D flip-flop.

$$Q = Clk\,D + Clk\,Qt - 1 \tag{6.2}$$

$$Q = Maj(Maj(Clk, D, 0), Maj(Clk, Qt - 1, 0), 1) \tag{6.3}$$

Table 6.1 Operation table for D type FF with clock input

CLK	Data Input	Qt	State
0	0	Qt-1	Hold
0	1	Qt-1	Hold
1	0	0	Transparent
1	1	1	Transparent

6.3.3 Proposed 2 Bit and N Bit Asynchronous Counter using Divide by 2 Counter

One of the useful features of D-type flip-flops is a binary divider for frequency division (or) as a divide by 2 counters. Here is the data input of D Flip-flop coupling to inverted output terminal Qbar. Here is the data input of D flip-flop coupling to inverted output terminal Qbar. It means that with the rising edge on the clock signal, the output will reach flip states. In this divide by 2 counter concepts, for the design of the counter, the first flip-flop

performs the division by 2 for the input clock frequency. This frequency is act as an output signal of the first flip-flop. The second flip-flop performs the division of input frequency by 2. That means division by 4 for the input frequency. Likewise, every flip-flop in counter circuits performs the division operation.

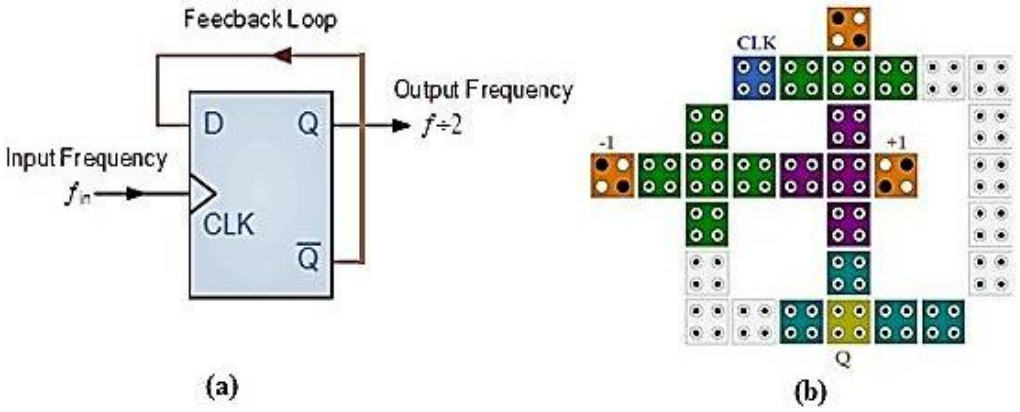


Figure 6.4 Divide by 2 counter (a) Logic diagram (b) QCA layout using D flip-flop

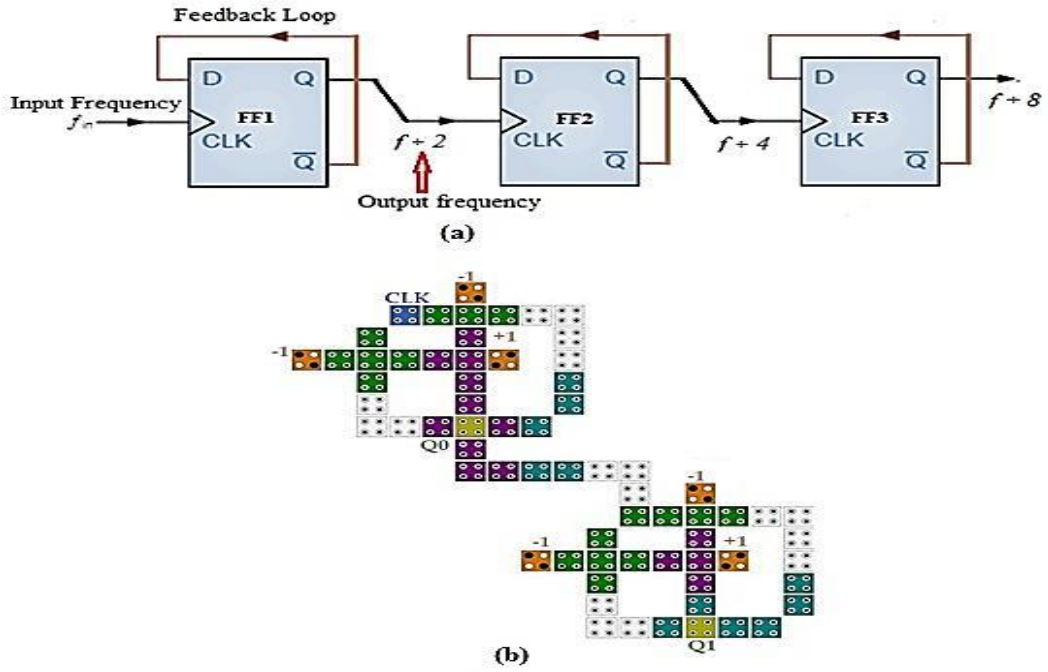


Figure 6.5 Asynchronous counter (a) Logic diagram (b) QCA layout for 2 bit counter using D flip-flop

Finally to get, the appropriate output signal across the output terminal of every flip-flop. This type of counter is called the asynchronous counter (or) ripple counter. Figure 6.4 (a) and Figure 6.4(b) show the logic diagram and QCA layout for dividing by 2 counter concepts using a D flip-flop. Figure 6.5(a) and Figure 6.5(b) show the logic for the asynchronous counter and QCA layout for the 2bit counter.

6.4 RESULT AND DISCUSSION

In this section, the proposed designs are simulated and verified the functionality and to access the overall figures of merit such as several QCA cells, area, latency, average energy dissipation, and simulation time. The simulation results of the proposed pulse generator, D flip-flop, and two-bit counter with input and output waveforms are verified using the QCA Designer tool. Based on the result the output of the D flip-flop was delayed after a 0.25 clock cycle with the input of the D flip-flop.

The polarization tends to provide a great value of ±9.87e-001at the output level. The simulation results of the proposed D flip-flop structures are compared with the prior design in terms of several cells, area occupation, latency, crossover type. Those parameters are highlighted in Table 6.2 for D-type flip flops and Table 6.3 for the 2bit counter. Among all the structures, the proposed structure of the D flip-flop is achieved less and the proposed 2 bit counter achieved a 30% improvement in terms of cell count and latency respectively. The comparison chart in terms of cells used and simulation time for the previous and proposed as shown in Figure 6.6.

Table 6.2 Comparison of QCA D-FF design by conventional matrices

Presented in	Cell count (*#cells)*	Area (μm^2)	Latency (10^{-12}s)	Average Energy dissipation (meV)	Simulation Time (Seconds)
(Vetteth *et al.* 2003)	66	0.08	1.5	2.57	57
(Hashemi & Navi 2012)	49	0.05	1	1.37	40
(Sabbaghi & Kianpour 2014)	36	0.04	1.25	1.70	28
(Goswami *et al.* 2014)	30	0.03	0.75	1.73	23
(Rezaei 2018)	45	0.04	0.75	1.39	38
(Abutaleb 2017)	28	0.02	0.5	1.44	23
Proposed D-FF	**22**	**0.02**	**0**	**0.782**	**19**

Table 6.3 Comparison of QCA Counter by Conventional Matrices

Presented in	Single Layer	Cell count(*#cells)*	Area(μm^2)	Latency(10^{-12}s)
(Xiaokuo *et al.* 2010)	Yes	616	1.2	5
(Sheikhfaal *et al.* 2015)	No	428	0.48	2
(Angizi *et al.* 2015)	No	287	0.33	2
Rezaei 2018	Yes	238	0.36	2.25
(Abutaleb 2017)	Yes	196	0.22	2
Proposed Counter	**Yes**	**111**	**0.29**	**0.5**

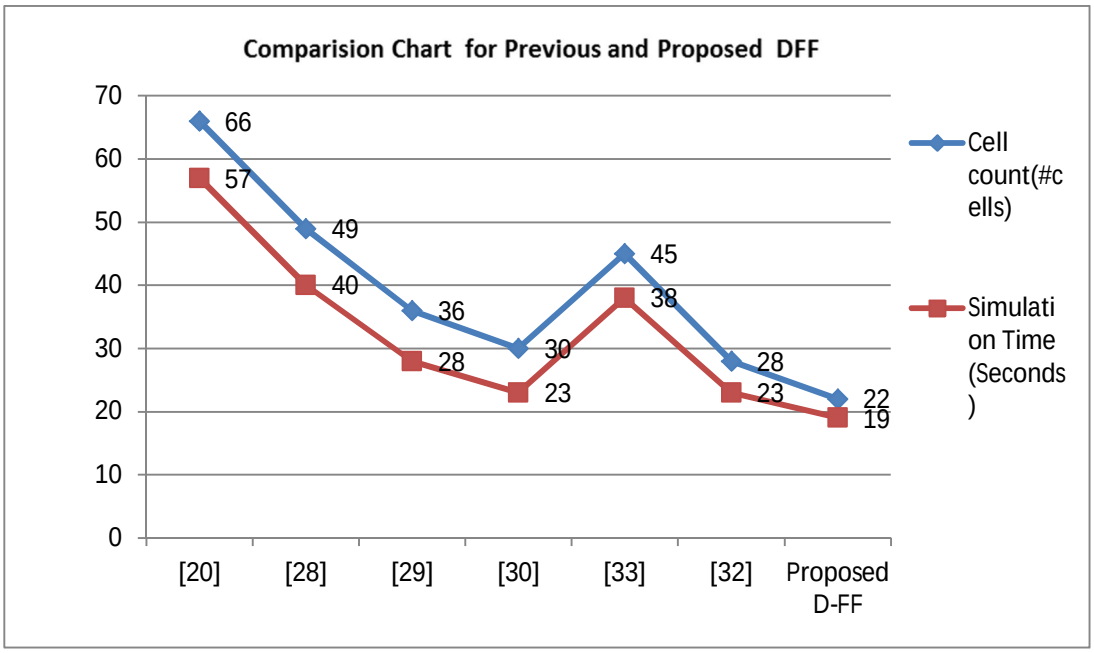


Figure 6.6 Comparison between Previous and Proposed D type FF

6.5 SUMMARY

In this work the efficient structures of a D flip-flop, 2 bit, and n bit asynchronous counter are proposed, simulated, and evaluated. All structures use a single layer with normal cells. In this proposed design without any crossover, to achieve the desired counter design. The design complexity is received when the use of divider by 2 counter concepts. From the simulation results the implemented work has fewer cells, minimum area coverage; increment in the polarization factor with a decrement in delay factor. The major use of the proposed work is in the construction of high-speed digital systems due to the decrement in power consumption and increment in performance analysis.

CHAPTER 7

A NOVEL DESIGN OF NANO ROUTER WITH HIGH-SPEED CROSSBAR SCHEDULER FOR DIGITAL SYSTEMS IN QCA PARADIGM

7.1 SCOPE AND OBJECTIVE

Energy loss is one of the challenging issues in designing circuits. Energy dissipation is proportional to the size of the device. The main aim is to search for a solution of small size with less power dissipation. A quantum dot cellular automaton is one of the promising solutions with less power and is small in size. At present one of the growing fields in research is QCA based on Nano communication.

In modern technology, everyone expects a high-speed data delivery router. It acts as a key element for data delivery. In this work, a new architecture on the router at the Nanoscale is proposed and implemented. The 4x4 Nano router implemented with modules 4:1 multiplexer, 1:4 demultiplexer, high-speed crossbar scheduler with a pulse generator, and 2-bit counter using D flip-flop and parallel to serial converter. The proposed research is to achieve Nano communication for high-speed data transmission.

7.2 RESEARCH METHODOLOGY

In this research work, router architecture for a high-speed crossbar scheduler with higher efficiency is presented and simulated using the QCA

designer tool. Various router designs in QCA technology have been considered for reference. In Das & Das (2012) majority gate-based data selector, cum router circuit is proposed. In (Sardinha *et al.* 2013), new router architecture is achieved at the receiver side with a demultiplexer and parallel to serial converter. In this design, multilayer crossover is utilized.

Various QCA layouts for the modules in router architecture like a multiplexer, demultiplexer, wire crossing techniques are proposed in (Iqbal *et al.* 2013, Shin *et al.* 2014). Using reversible gate to achieve Nano communication in Das (2016). The efficient design of multiplexer for crossbar arbiter design is proposed in (Thakur *et al.* 2016) using QCA technology. For high-speed applications, the on-chip crossbar scheduler can be proposed and implemented in (Thakur *et al.* 2018).This proposed structure can be implemented and compared in both CMOS technology and QCA technology. In (Kamaraj *et al.* 2019) the reversible logic with a space-efficient Nano router is presented. This research paper utilized a multilayer cross-over structure.

7.3 PROPOSED WORK

A router is a leading device in the present communication period. A router is a networking device that forward data between computer networks. The router performs the traffic directing functions on the internet. Data sent through the internet, such as a webpage (or) email, is in the form of data packets. A packet is typically forwarded from one router to another router through the networks that constitute an internetwork until it reaches its destination node. To achieve a Nano communication system with a Nano router at Nanoscale circuits in this work.

7.3.1 Importance and Design Parts of Nano Router

The Nano router is small in size. Despite its tiny size, the Nano router offers more wireless functions than many regular-size routers. It can be used as a router, an access point, a range extender, or a media bridge. Its best, and default, use it as an access point for those wanting to quickly add wireless clients to an existing wired network, such as that of a hotel room. That plus the ultra-compact size makes the router a useful companion for mobile users. As these routers are more compact it's more portable where a user can easily use the router wherever they want.

This Nano router is designed for its small size and ultra-speed data transfer. Moreover, these routers exhibit higher data transfer speeds than the conventional ones. Present routers are huge and the data transfer speed varies based on the router design, but these Nano routers are tiny thus their size makes them more portable such that a user can take the router on the go. The range covered by the Nano router is comparatively high and its performance is also greater than the conventional one. The advantage of the Nano routers are its can be easily used as other devices also such as routers, access points, range extenders, media bridges, etc.

The cost of the Nano router is considerably lower than the conventional one. These Nano routers can be used as a travel router due to their compact size. The designed Nano router uses simple functionality rather than complex one yet these simple functionalities make the Nano routers more portable and efficient than the conventional routers.

The router has two majority functional units; they are a memory block and a router block. The memory block consists of a decoder, memory array, multistage interconnection network, and multiplexer. The router block has a demultiplexer, switch fabric, and parallel to serial converter as shown in Figure 7.1. The integral specifications of the router are listed in Table 7.1.

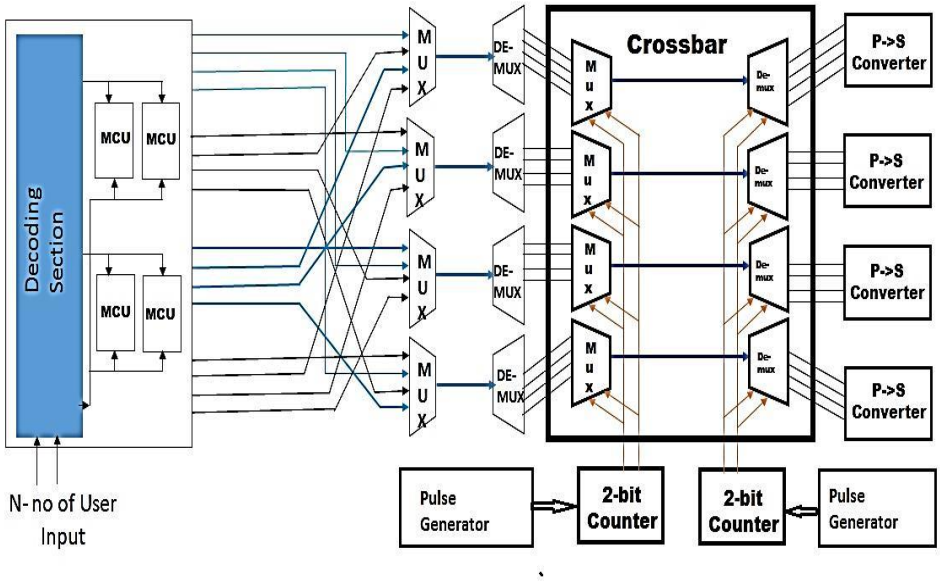


Figure 7.1 The proposed structure of the Nano router

Table 7.1 Particularization of the nano router

S.No	Components of Nano router	Specification
1	Decoder	2 to 4
2	Memory Array	4x4
3	Multiplexer	4x1
4	Demultiplexer	1x4
5	Parallel to serial converter	4 to 1
6	Switch fabric	4x4

7.3.2 Design of Router Modules

7.3.2.1 Proposed two-bit counter with pulse generator

In this Nano router architecture, the switch fabric is connected with a two-bit counter using D type flipflop. The clock signal is important for the operation of sequential circuits Pulse generator produces pulses instead of the clock signal for this high-speed scheduler design.

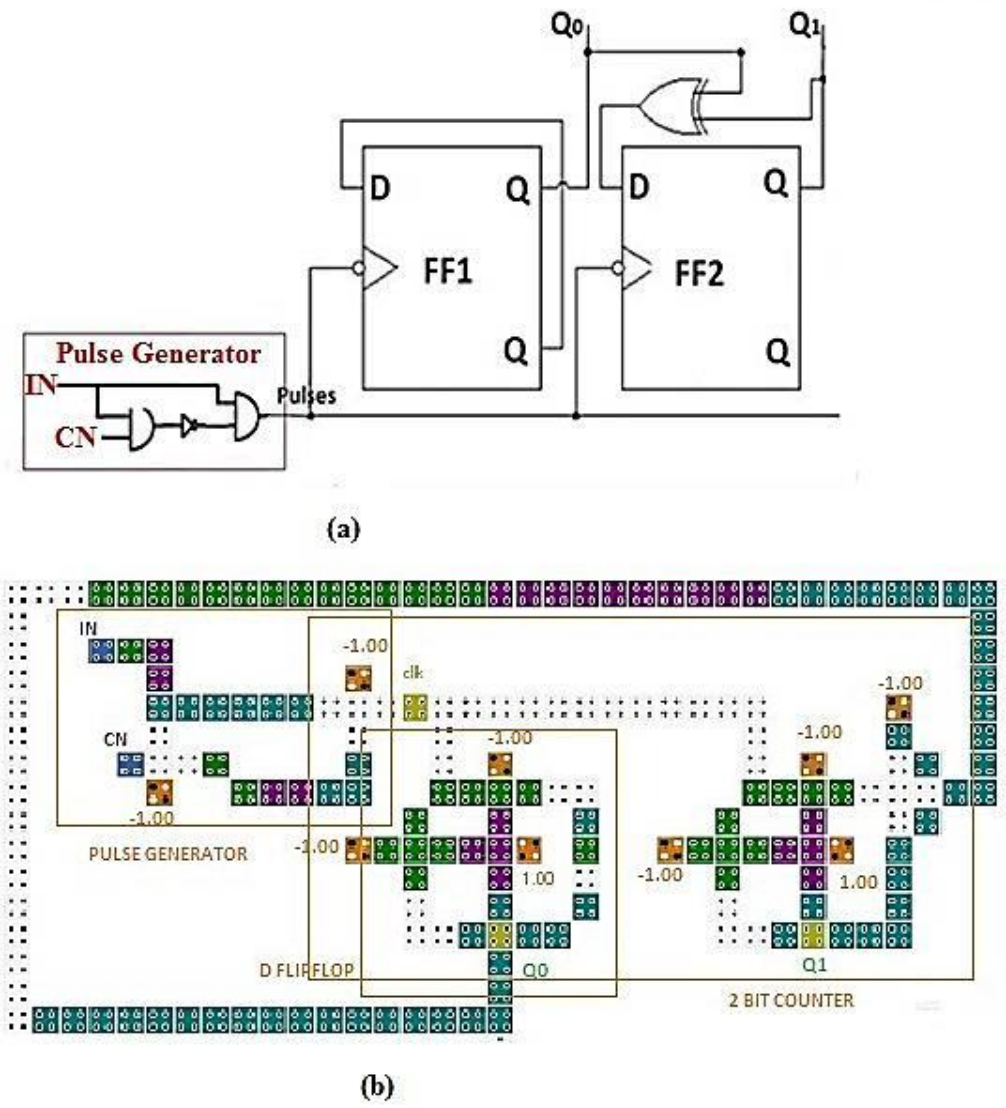


Figure 7.2 Proposed two-bit counter (a) Logic diagram (b) QCA layout

It is designed based on a majority gate with two inputs IN and CN. This circuit produces pulses when the input is set by IN=1 and CN=0. For the remaining combinations, the output of the pulse generator is zero. The proposed architecture of the pulse generator and D flip-flop logic diagram and QCA layout is discussed in chapter 5.For 2 bit counter design designed for the switch fabric in Nano router architecture by D flip-flop and two-input exclusive OR gates. Figures 7.2 (a) and (b) shows the logic and QCA layout diagram for the proposed 2 bit counter using a D flip-flop.

7.3.2.2 Design of 4x1 multiplexer

A multiplexer is known as a data selector in communication systems. It is a device that selects data between several input data and forwards it to a single output line. The selection of the output depends on the selection input. Generally, multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. The functionality of the multiplexer can be understood with the help of equation 7.1.

$$Out\ Y = S0'S1'I0 + S0'S1I1 + S0S1'I2 + S0S1I3 \quad (7.1)$$

The proposed structure of the multiplexer is developed using a majority gate. In this design nine majority gates and one inverter can be utilized. Figure 7.3 (a), 7.3 (b), and 7.3 (c) shows the schematic diagram, majority gate-based logic diagram, and QCA layout for the proposed 4x1 multiplexer.

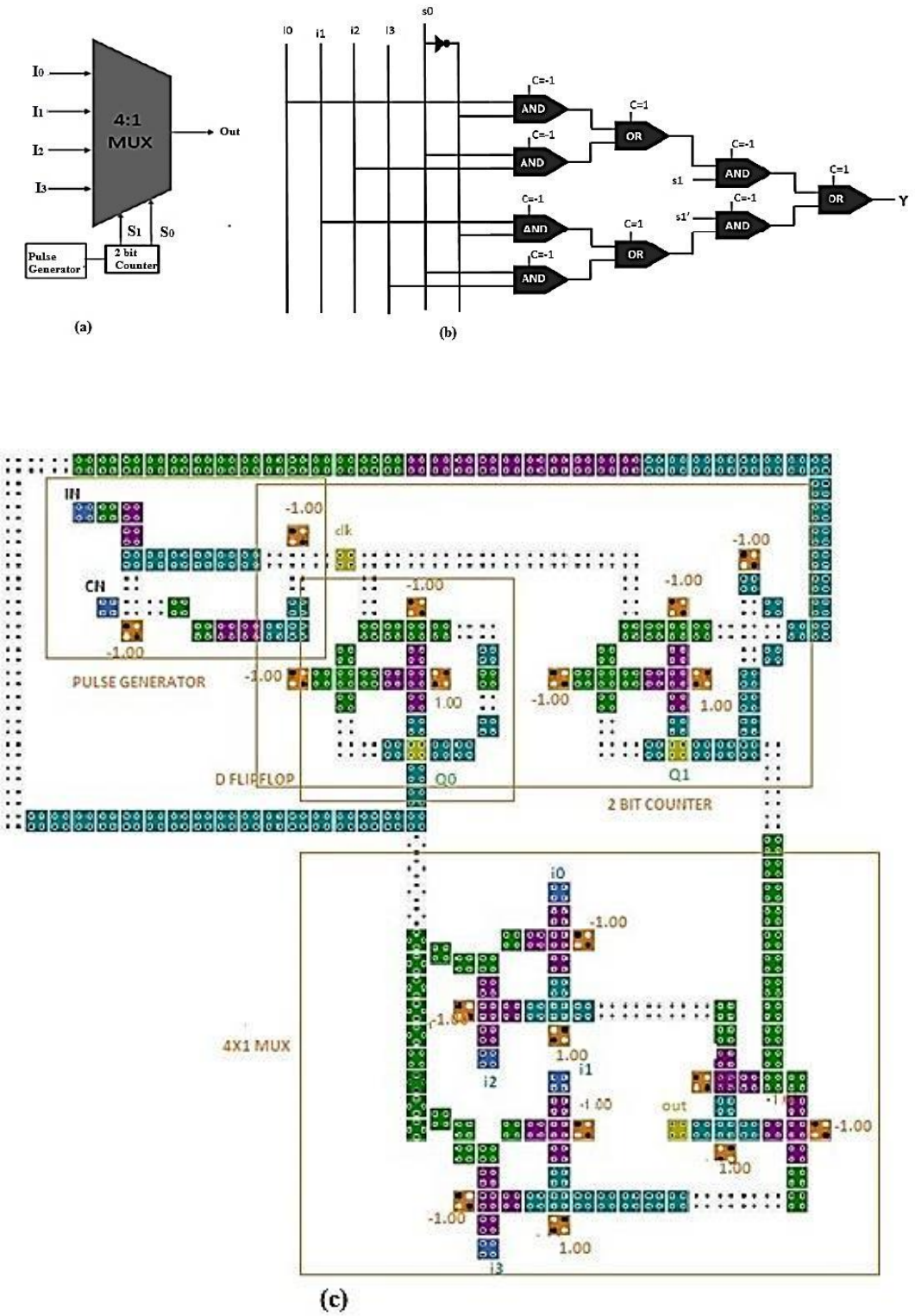


Figure 7.3 Proposed design of 4x1 multiplexer (a) Logic diagram (b) Majority gate based design (c) QCA layout

7.3.2.3 Design of 1x4 demultiplexer

A demultiplexer is a device that takes a single input line and routes it to one of several digital output lines. It is commonly known as a data distributor in communication systems. Based on selection input the unique input data is sent towards any one of the output lines. In the Nano router architecture, the demultiplexer output is connected to the parallel to serial converter. To build a 4x4 Nano router utilized a 1x4 demultiplexer. The logic diagram, majority gate-based circuit, and QCA structures are shown in Figures 7.4. The functionality of the demultiplexer can be recognized through the equation 7.2 to 7.5.

$$P = Maj(Maj(S0', Input, 0), S1', 0) \tag{7.2}$$

$$Q = Maj(Maj(S0', Input, 0), S1, 0) \tag{7.3}$$

$$R = Maj(Maj(S0, Input, 0), S1', 0) \tag{7.4}$$

$$S = Maj(Maj(S0, Input, 0), S1, 0) \tag{7.5}$$

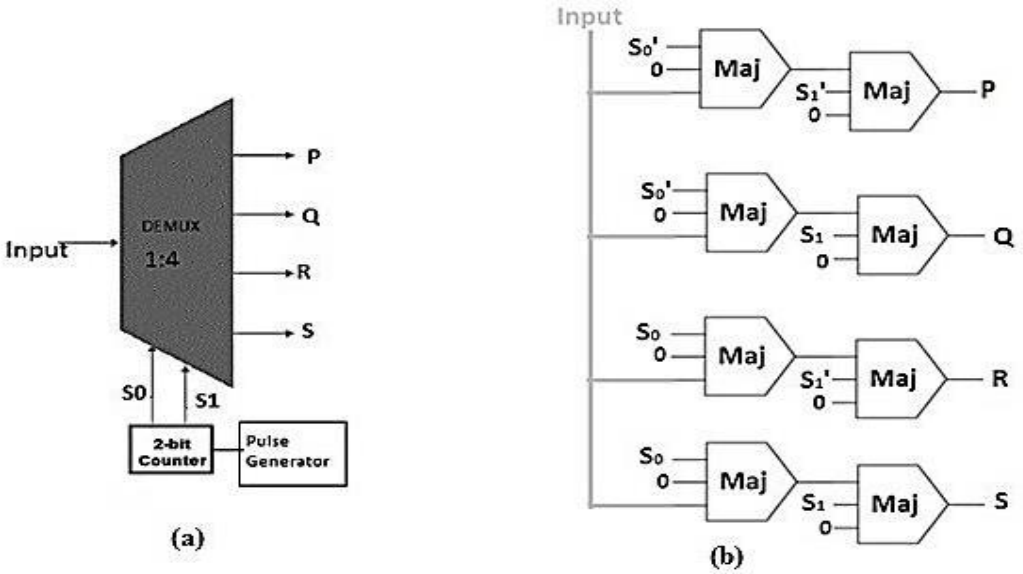


Figure 7.4 (Continued)

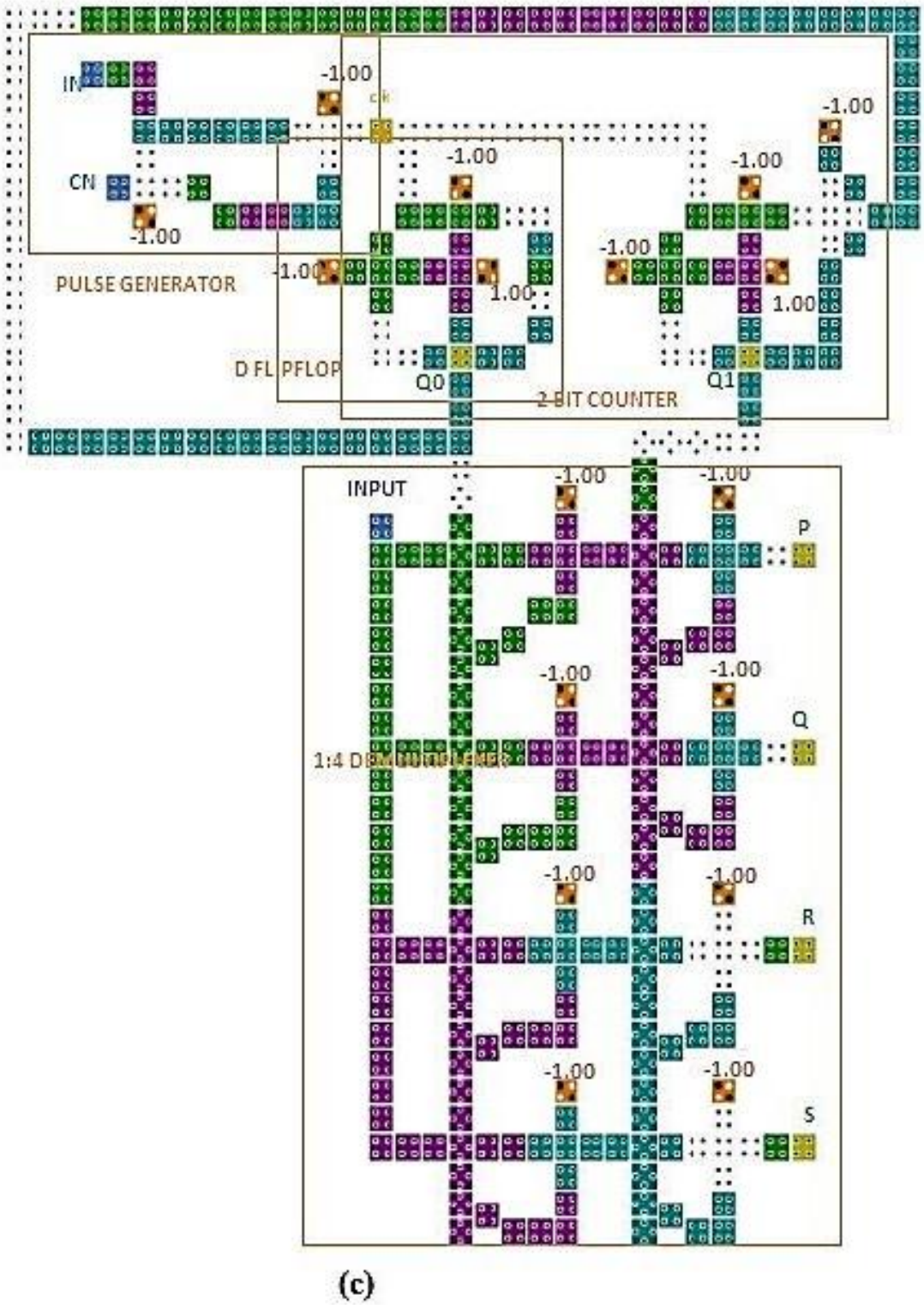


Figure 7.4 Proposed design of 1x4 demultiplexer (a) Logic diagram (b) Majority gate based design (c) QCA layout

In parallel to serial converter, all the parallel data is loaded simultaneously into 4 bit parallel in serial-out shift register using D flip-flop. The output of the converter arrives at different instants of time. The QCA layout structure is already proposed in (Kamaraj *et al.* 2020).

7.3.2.4 Design of proposed 4x4 nano router

In the previous sections, the major components of the router are realized in the QCA environment and their functionality is verified by a single router with one 4x1 multiplexer, one 1x4 demultiplexer, and one parallel to serial converter in the QCA environment as shown in Figure 7.5. The crossover structure of the multilayer configuration is indicated earlier. With a QCA environment, a 4x4 Nano router is designed with all router modules as shown in Figure 7.6. To achieves a high-speed Nano router for Nano communication.

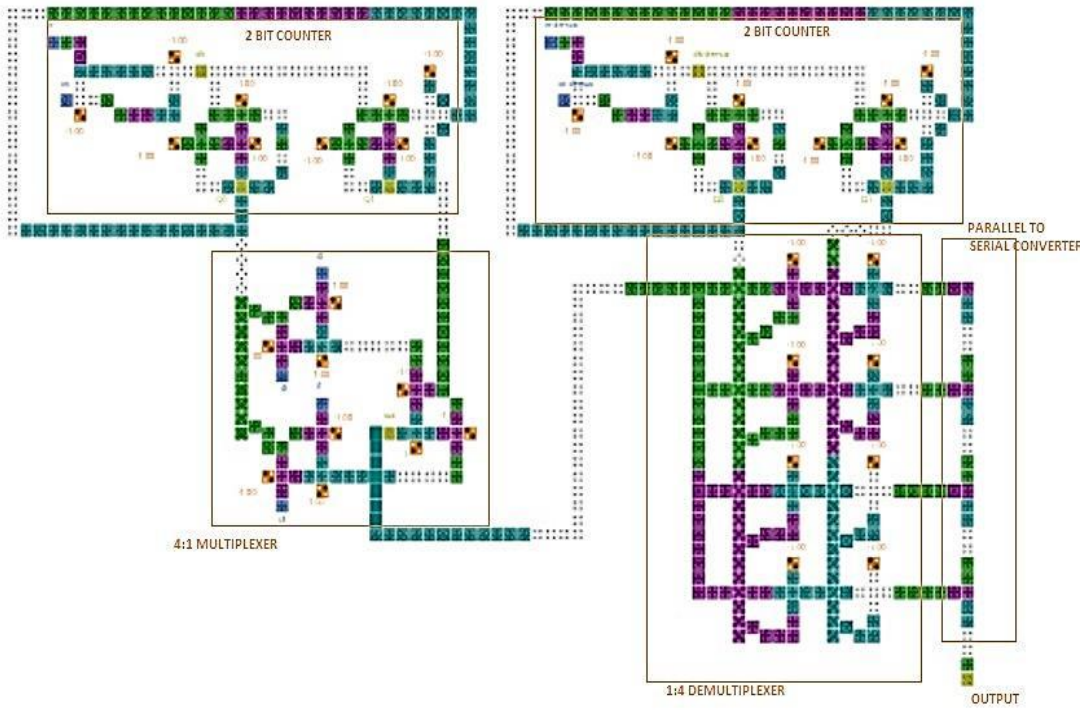


Figure 7.5 Proposed QCA layout for the single Nano router

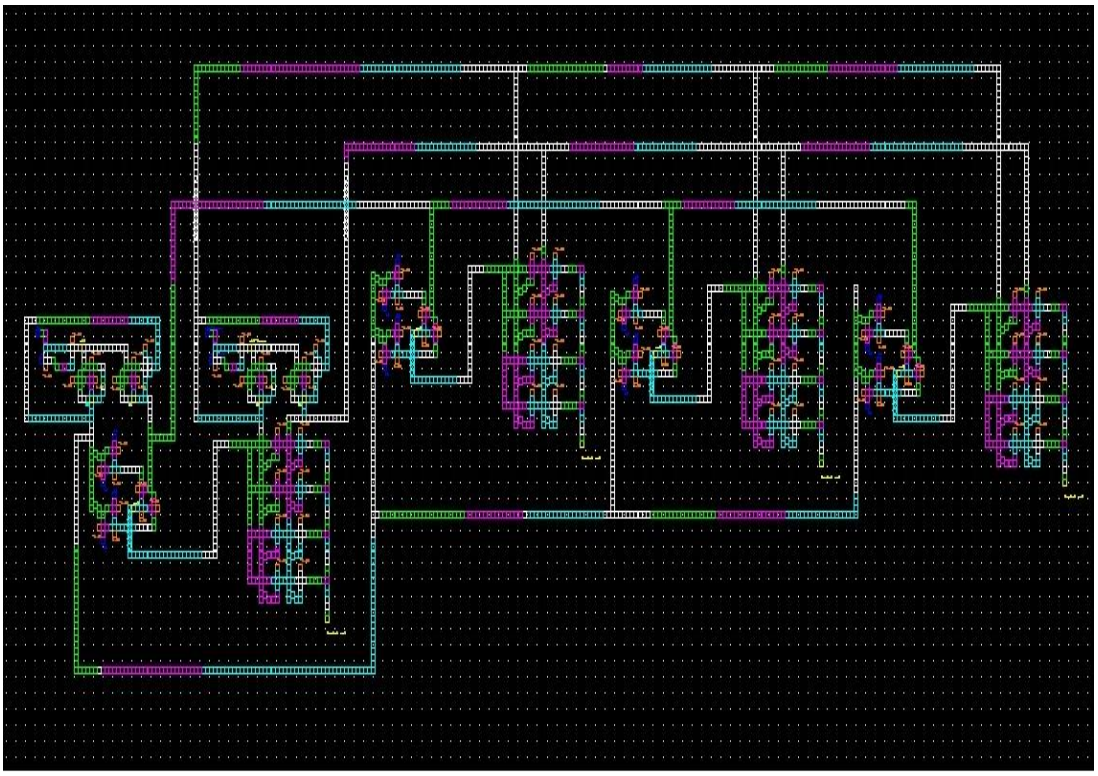


Figure 7.6 Proposed QCA layout for the 4x4 Nano router

7.3.2.5 Router implementation in Xilinx environment

It has been shown in this study that the suggested structure of 4x4 Nano routers with a crossbar scheduler can be replicated in the Verilog and Xilinx environments. It has been implemented in Verilog to mimic the proposed 4x4 Nano router and crossbar planer in the Xilinx domain, as well as in other fields. The scheduler's Register Transfer Level architecture and circuit layout, as seen in Figures 7.7 and 7.8, are illustrated in the following ways: Arbiters are electronic devices that assign access to shared resources on a computerized basis.

Several arrangements still exist in which a large number of requesters must get access to shared assets. Typical resources include shared memory, switch fabrics, skilled state machines, and multiplexed configurable

elements. They may be any combination of these. An arbitrator is required to maintain control over how the resource is split among several suppliants. Round robin token transitory buses or switch arbiters assure that masters are not biased against one another, and they also allow any new time slot to be committed to a master who is late for his or her round-robin turn but is ready now. The round-robin approach is desirable because it provides an accurate estimate of worst-case waiting times.

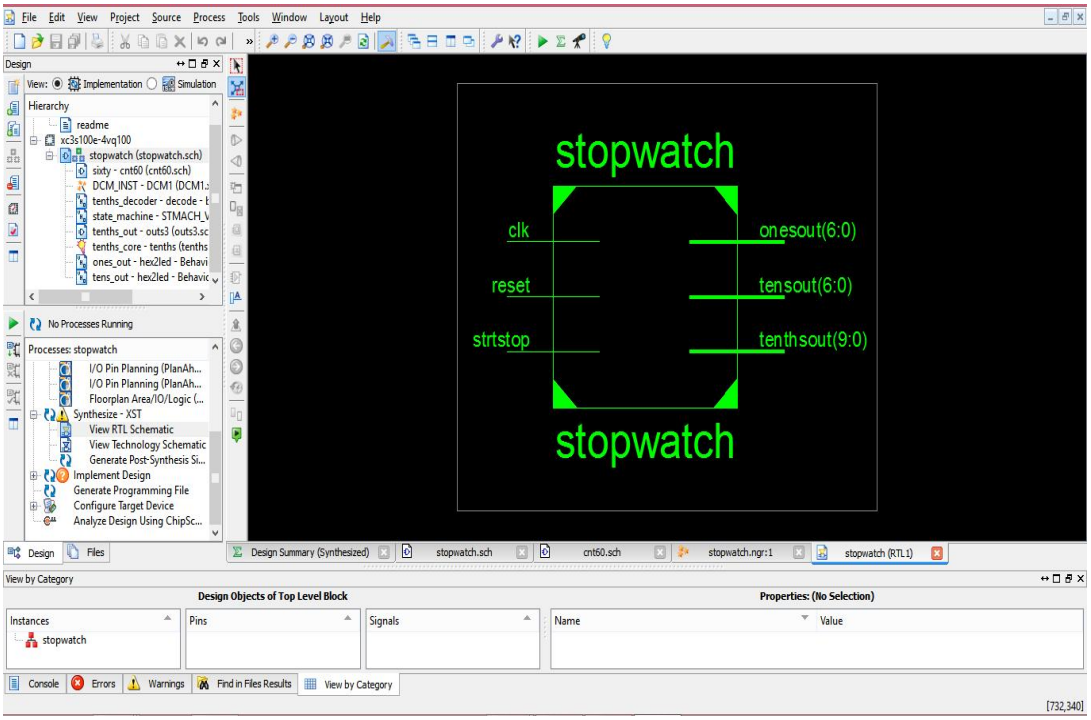


Figure 7.7 The RTL schematic for the proposed 4x4 Nano router in the Xilinx environment

A common characteristic of all patterns is that one of the masters has an undue preference for entrance to a shared asset, which is followed by the convention of a round-robin token passing bus or switch arbiter. The main with the next excessive preference that sends an appeal can be granted access to the resources, and the master with the highest importance can then transfer the token to the next master in round-robin order because the master who

holds the ticket does not require the resources during this cycle. Figure 7.9 depicts the simulation result for the Xilinx Verilog environment using the Nano router as an example.

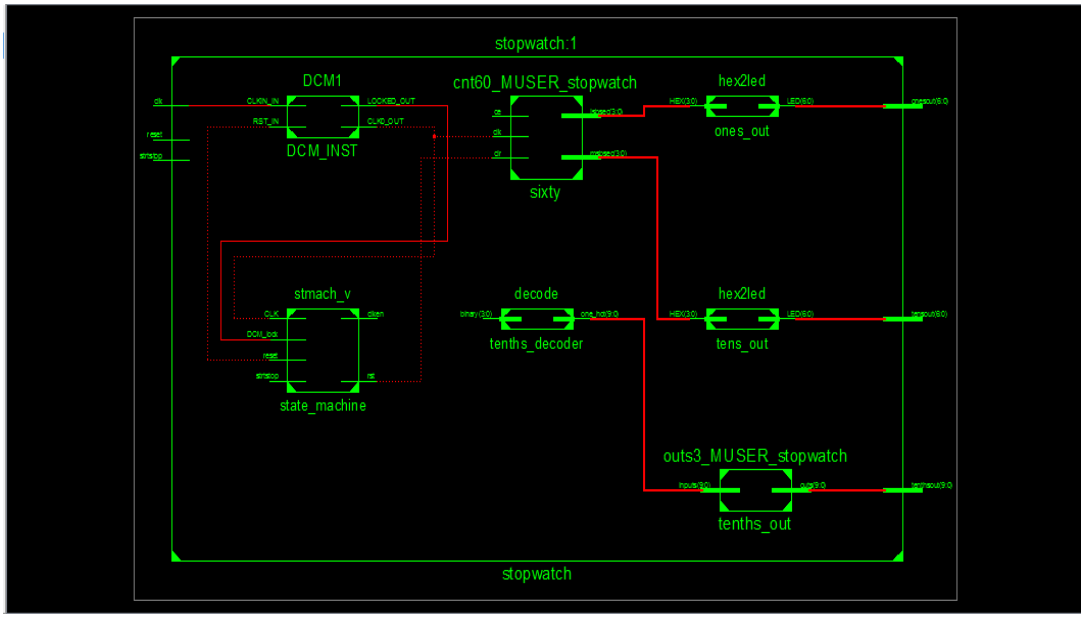


Figure 7.8 The circuit diagram for the proposed 4x4 Nano router in the Xilinx environment

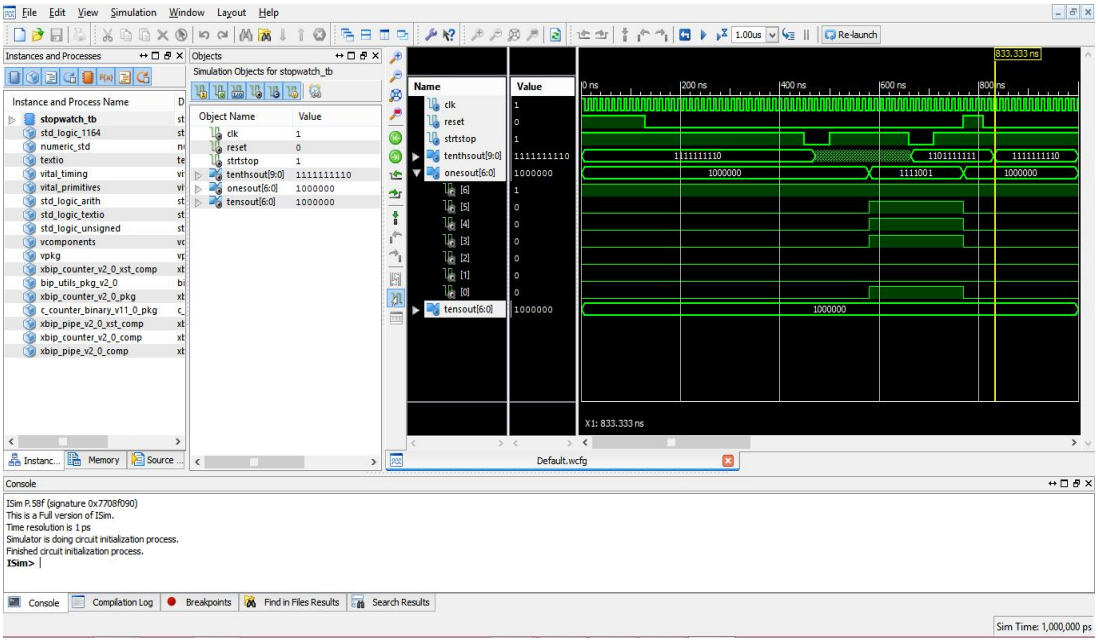


Figure 7.9 The simulation output for the proposed 4x4 Nano router in the Xilinx environment

7.4 RESULT AND DISCUSSION

The implementation and simulation of proposed circuits are achieved by using the coherence vector simulator in QCA designer 2.0.3. The simulation is carried out by the Euler method. The parameters for the coherence vector are considered and tabled in Table 7.2.

Table 7.2 Coherence vector parameters model

S.No	Parameter	Value
1	Time Step	1.000000e-016 s
2	Total Simulation Time	7.000000e-011 s
3	Clock High	9.800000e-022 J
4	Cell Size	18nm
5	Clock Low	3.800000e-023J
6	Relaxation time	4.1356675e-14 s
7	Clock shift	0.000000e+000
8	Temperature	1.000000 K
9	Clock Amplitude Factor	2.000000
10	Relative Permittivity	12.900000
11	Radius of Effect	80.000000 nm
12	Layer Separation	11.500000 nm

7.4.1 Simulation Result for D Flip-Flop with Pulse Generator

The functionality of the D flip-flop with the pulse generator is verified using the simulation result. The data input of D input data is transferred towards output for the generation of pulses. Figure 7.10, Figure 7.11 shows the simulation result for the Pulse generator and D flip-flop with

the pulse generator. Figure 7.12 shows the simulation result for the 2 bit counter.

7.4.2 Simulation Result for 1x4 Multiplexer with 2 Bit Counter

Figure 7.13 shows the simulation result for a 1x4 multiplexer with the two-bit counter. The data input for the multiplexer is transferred towards the output by the selection of the selection input. The selection input is generated by the two bot counter. The functionality of the multiplexer is verified using simulation.

7.4.3 Simulation Result for 4x1 Multiplexer with 2 Bit Counter

The data input for the demultiplexer is transferred towards the output line by the selection of selection input. The opposite function of a multiplexer can be done by the demultiplexer. It performs data distribution towards the output. Figure 7.14 shows the functional verification of the proposed 4x1 demultiplexer with a two-bit counter operation.

7.4.4 Simulation Result for Single Nano Router

Figure 7.15 shows the simulation result for a single Nano router with the module of one 4x1 multiplexer,1x4 demultiplexer, and parallel to serial converter. The functionality of transferring the data packets from one end to another end can be varied and tested by the simulation result.

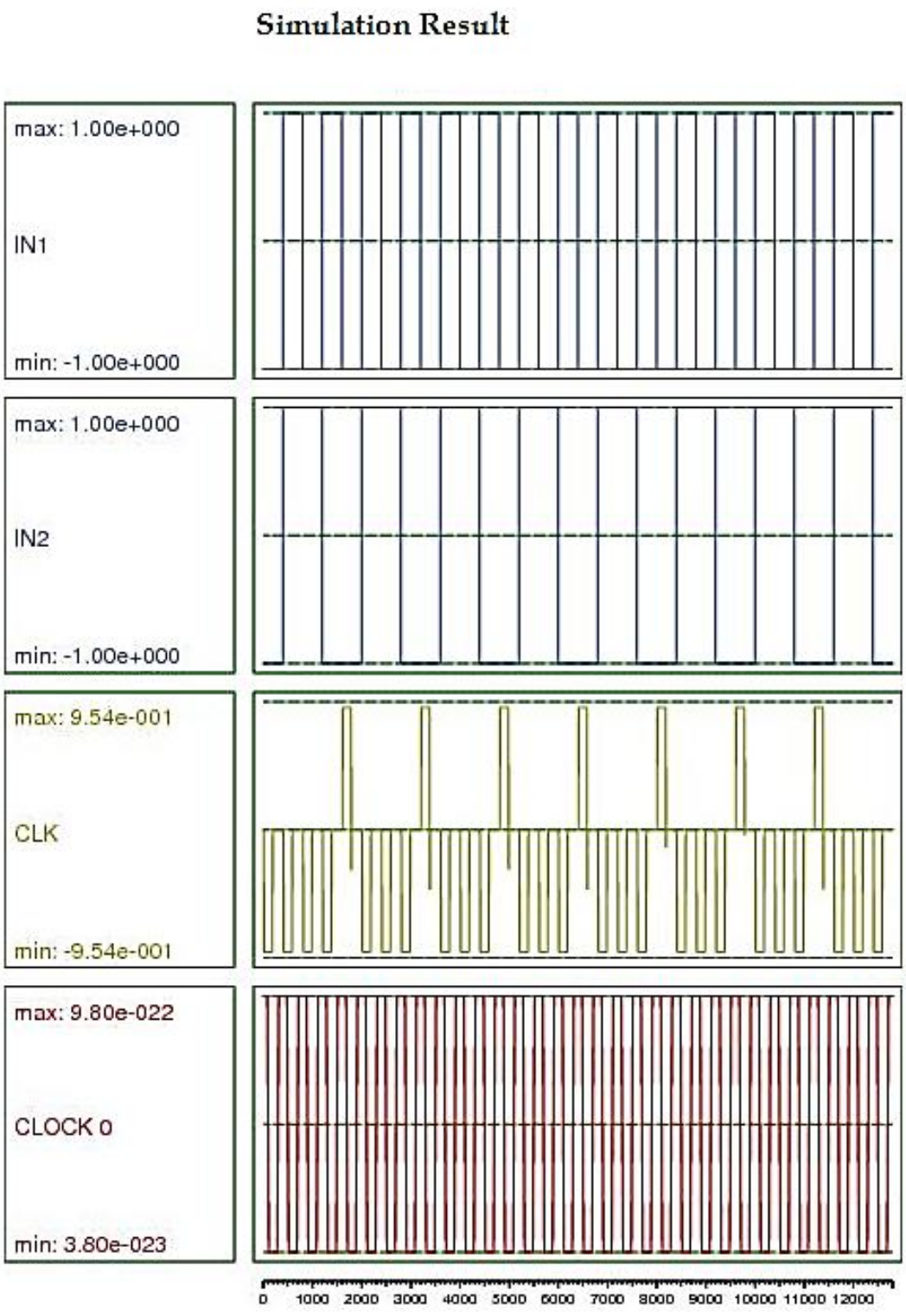


Figure 7.10 Simulation Result for Pulse Generator

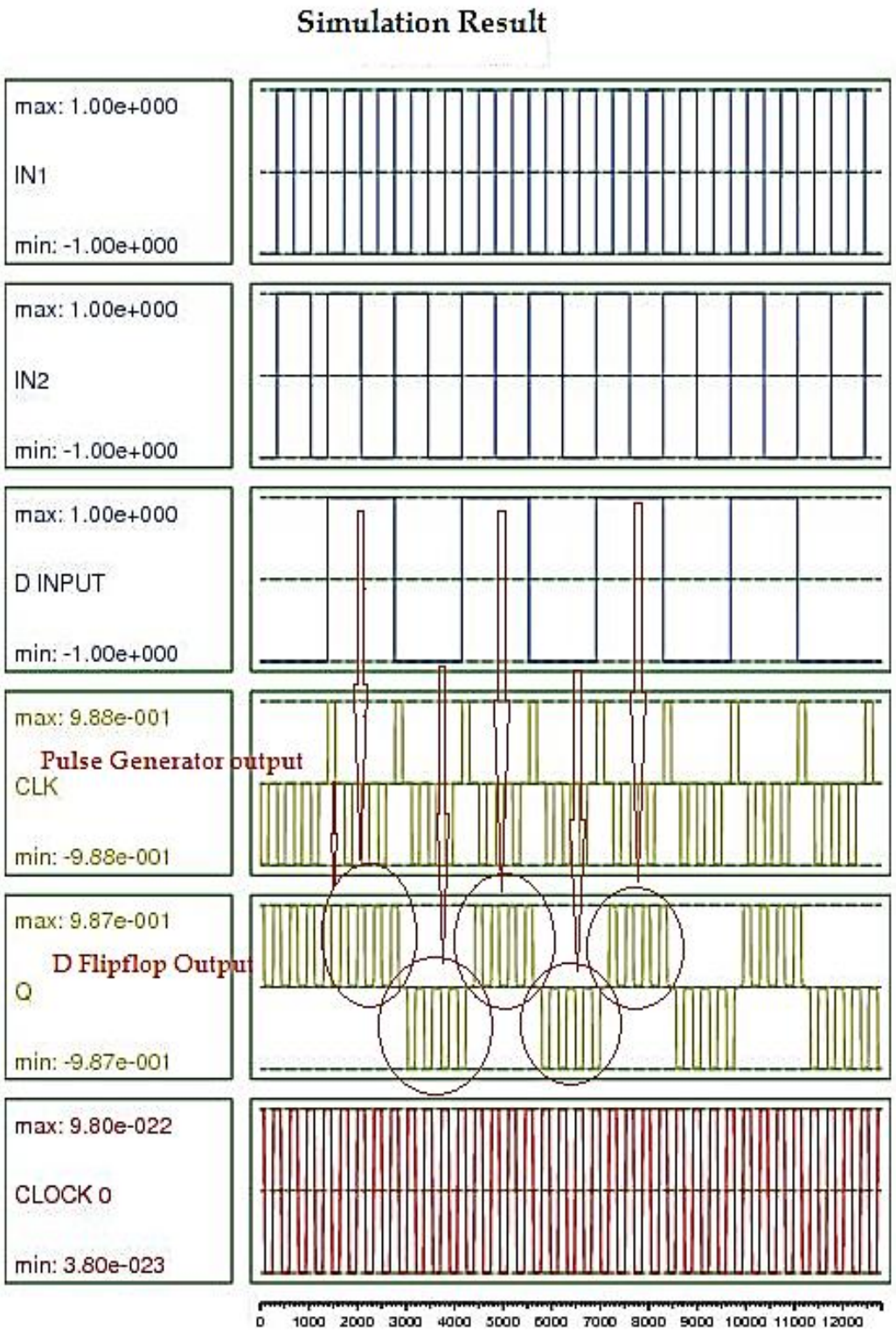


Figure 7.11 Simulation Result for D Flip-flop with Pulse Generator

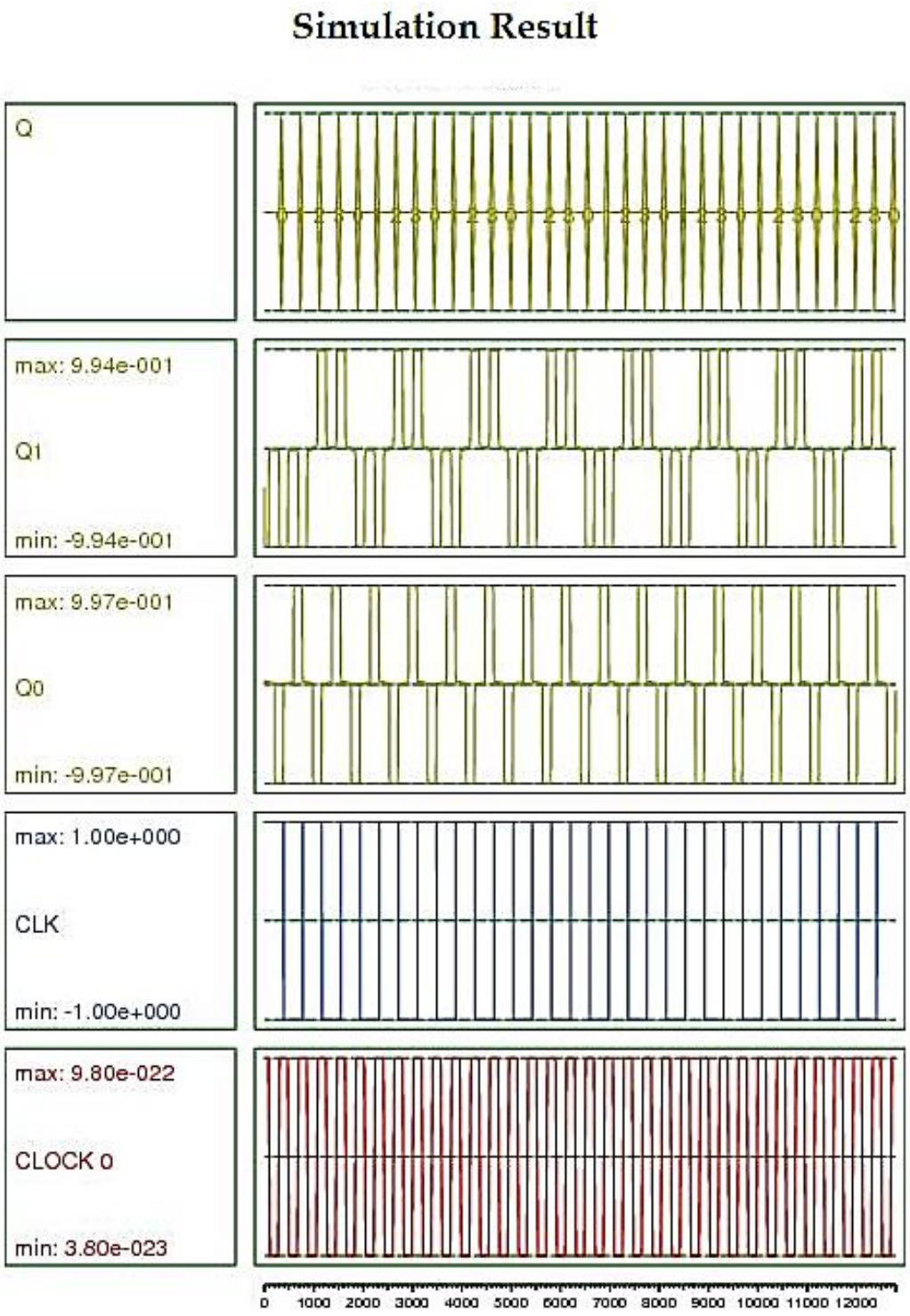


Figure 7.12 Simulation Result for 2 bit counter using proposed D Flip-flop

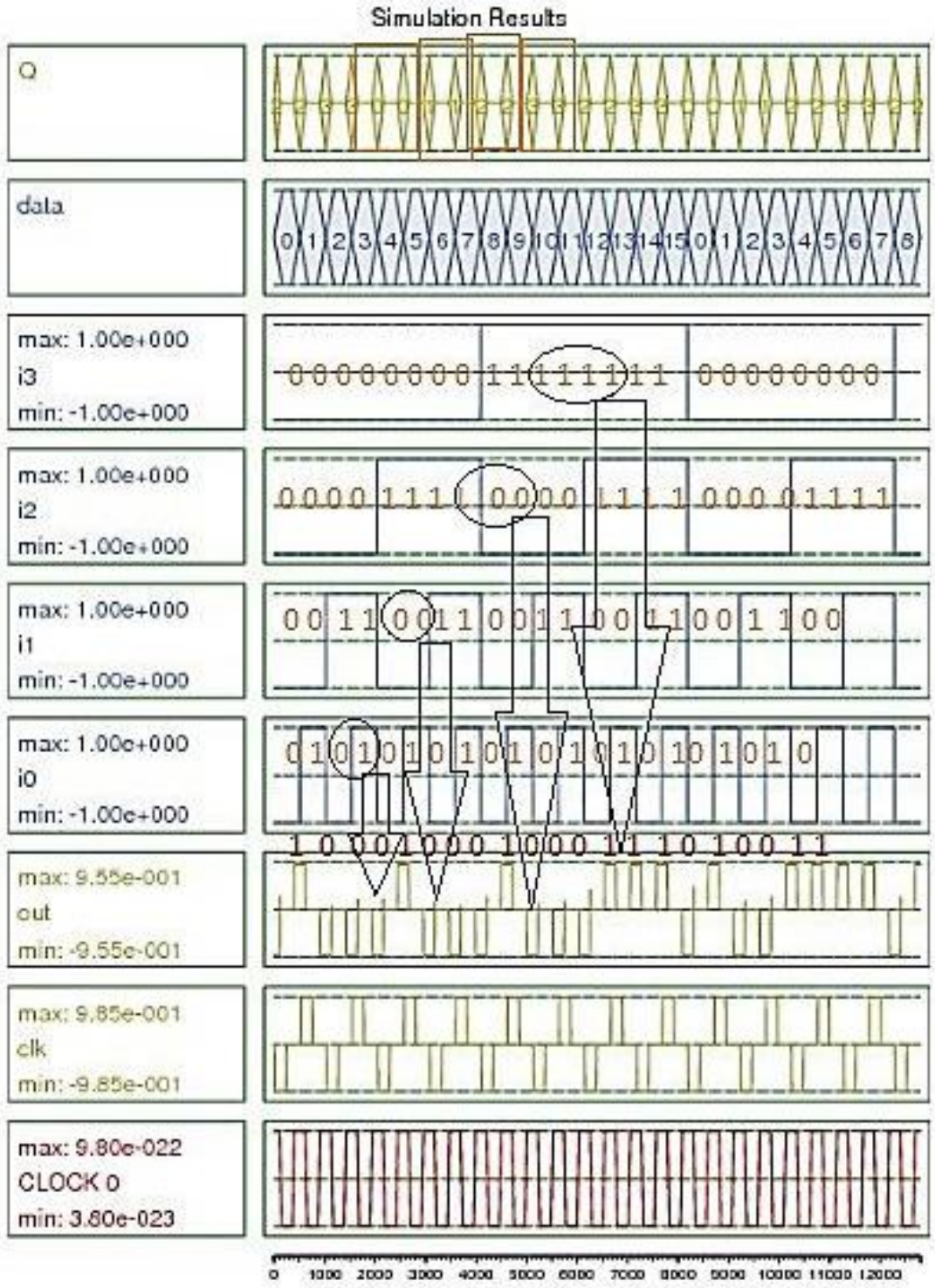


Figure 7.13 Simulation Result for 4:1 multiplexer

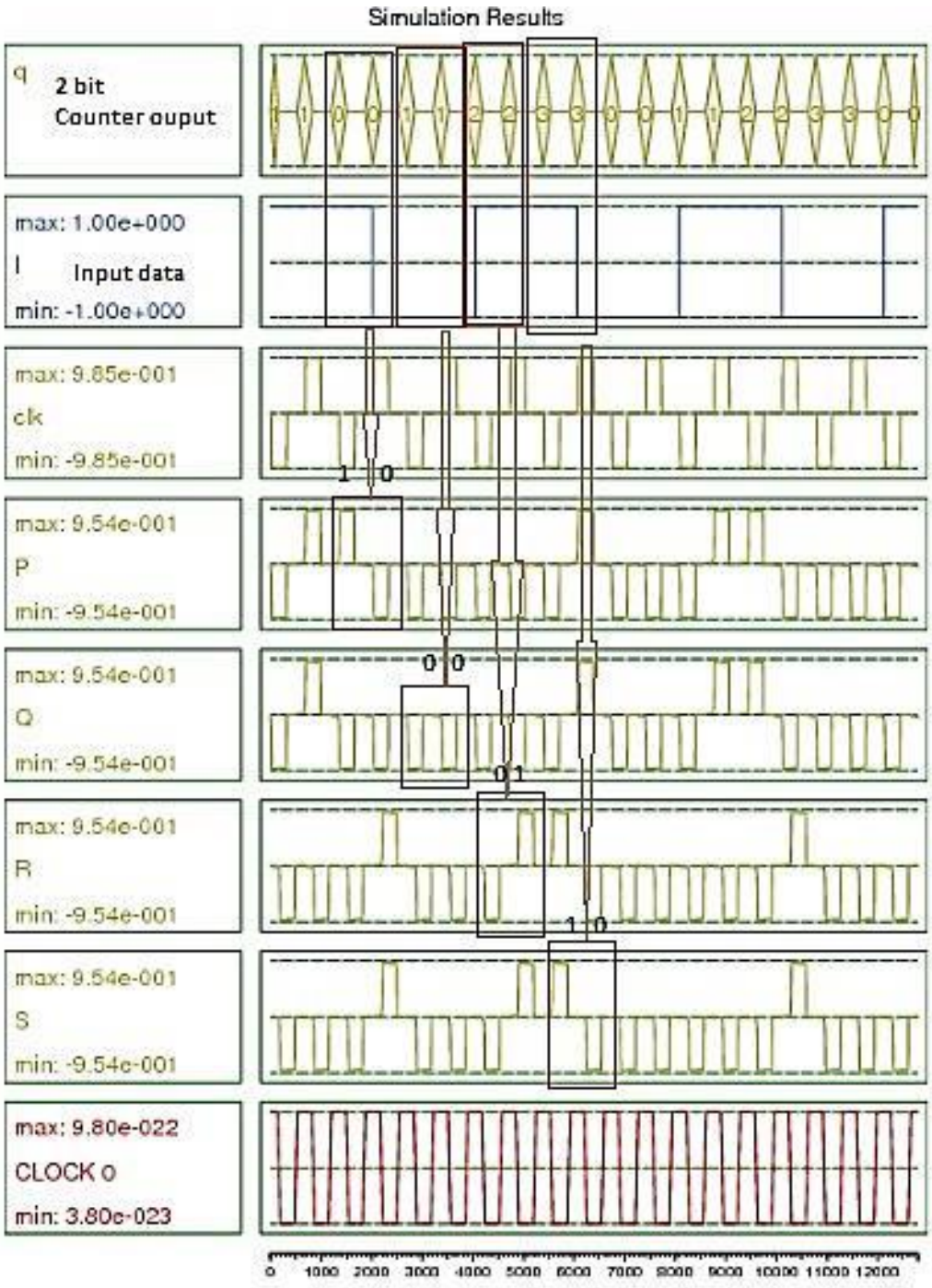


Figure 7.14 Simulation Result for 1:4 demultiplexer

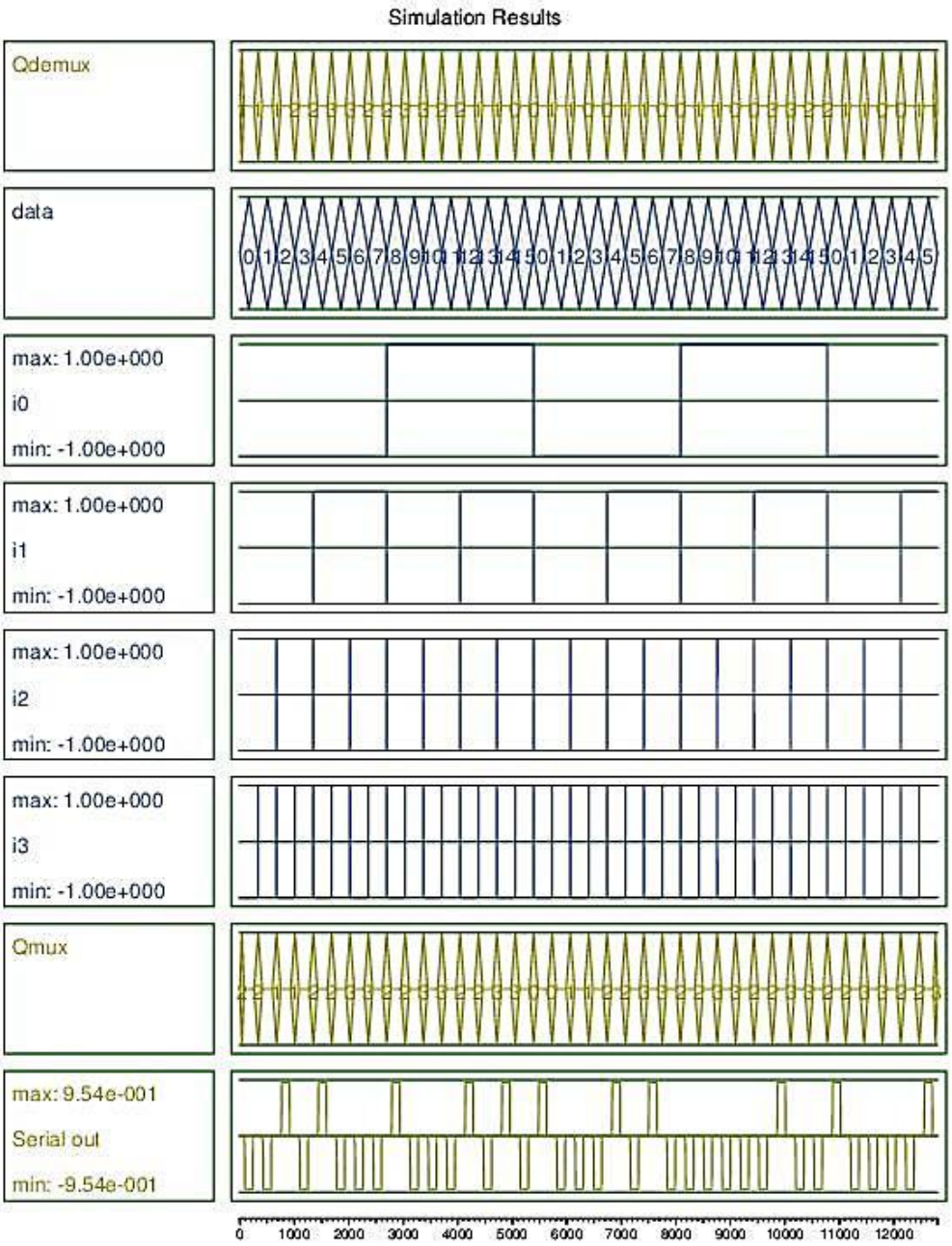


Figure 7.15 Simulation Result for proposed single Nano router

The performance matrices of the proposed single router with various modules are analyzed in Table 7.3. The power analysis can be done for the proposed design using the QCA Designer E tool and the different performance matrices are analyzed and compared in Table 7.4 for single and 4x4 nano routers. Also, the result can be reached in both the QCA environment and the Xilinx environment.

Table 7.3 Various analysis parameters of the proposed Nano router in QCA technology

S.No	Design Block	Type of Implementation	Gate count	Cell count (*#cells*)	Area (μm^2)	Latency (10^{-12}s)	Crossover Type
1.	Pulse Generator	Using 3 Input MG	2	21	0.02	0	Single-layer
2.	D-Flip-flop	Using 3 Input MG	3	22	0.02	0	Single-layer
3.	4:1 MUX	Using 3 Input MG	9	87	0.15	0.15	Single-layer
4.	1:4 DEMUX	Using 3 Input MG	8	205	0.25	0.15	Coplanar Crossover
5.	Crossbar Scheduler	Using 3 Input MG	25	734	1.51	1.00	Coplanar Crossover
6.	4X4 Nano router	Using 3 Input MG	100	3693	8.09	0.15	Coplanar Crossover

Table 7.4 Comparison for the proposed design in Xilinx and QCA environment

QCA Environment					
Design Block	**Cell count (*#cells)***	**Area (μm^2)**	**Latency (10^{-12}s)**	**Total Energy Dissipation (Sum_Ebath)**	**Average Energy Dissipation per cycle (Avg_Ebath)**
Router(4x4-Only Demux and Parallel to serial converter) existing design (Sardinha *et al.* 2013)	4026	13.81	48	-	-
Router (4x4 Router design) existing design (Kamaraj *et al.* 2020)	3057	7.91	24	-	-
Router(4x4-Only Demux and Parallel to serial converter) existing design (Das *et al.* 2017)	3551	9.86	15	-	-
Reversible Router (Single router) existing design (Das *et al.* 2013)	1388	19·77	20	-	-
Proposed Router (Single Router)	774	1.51	14	2.82e-001 eV (Er: +/- -2.47 e^{-002} eV)	2.56e-002 eV (Er: +/- -2.24 e^{-003} eV)
Xilinx environment					
Methods	**Pieces**	**Delay (ns)**	**Frequency (MHz)**	**Power (W)**	
Priority Based Router (Existing)	1342	12.6	74.07	1.44	
Address Based Router (Proposed)	123	7.841	112.116	0.420	

7.5 POWER ANALYSIS

The QCADesigner-E tool has one more special simulation engine available for the calculation of Energy dissipation in eV, name as Coherence vector energy engine (w/Energy). This tool is a reformed version of QCA Designer ver 2.0.3 tool. This tool is helping in calculating the energy dissipation for QCA circuits .In this tool involved coherence vector, bistable approximation and coherence vector (w/Energy) setups for simulation. Those three different simulation engine setups are used to find the energy dissipation in path. Hamiltonian matrix is used to calculate the energy and power of the QCA circuits for two state systems.

In this work, the energy dissipation for the proposed circuit is analyzed by using the QCADesigner-E tool. For simulation used the coherence vector simulation engine setup (w/Energy). Low saturation energy and high saturation energy of clock signal are the main parameters of coherence vector simulation engine setup. The values are 3.8e-23 J and 9.8e-22 J respectively. In this work , measured 18 nm × 18 nm is the regular cell size of QCA cell, 5 nm as a quantum dot-diameter and 20 nm is the distance between two quantum cells is for single layer design. And other measurements are total simulation time is 80e-15 s, the period of input signals is 10e-12 s and interval of each iteration step is1e-17 s. To achieve the low power dissipation and high-speed data transfer from different incoming links to various outgoing links by the design of the Nano router and realizing the circuit in quantum-dot cellular automata.

The designed Nano router structure is realized in the QCA platform with multilayer architecture for wire crossing. The designed 1:4 multiplexer requires 9 Majority gates, one inverter with the utilization of 90 cells, and area coverage is 0.13μm2. The proposed 4:1 demultiplexer consists of 192 cells, 8 majority gates with 0.19μm2 area coverage. The 2 bit counter uses a D flip-flop designed with 85 compartments, one two-input exclusive OR gate, and it occupies a 0.09 μm2 area. The pulse generator is designed with 3 majority gates, 27 cells with a 0.04 μm2 area. The single router is designed with 25 majority gates with 734 cells and it occupies a 1.51 μm2 space. Also, it utilized multilayer crossover for getting the correct output. The 4x4 Nano router uses 100 majority gates with 3693cells. The energy dissipation for the whole design is calculated and tabulated in Table 7.4. The total error of QCA cell is zero over an entire clock cycle of all energy movements is demonstrated in equation 7.6.

$$Error = Ebath - (Eclock + EIO) \tag{7.6}$$

7.6 SUMMARY

To achieve the low power dissipation and high-speed data transfer from different incoming links to various outgoing links by the design of the Nano router and realizing the circuit in quantum-dot cellular automata. The designed Nano router structure is discovered in the QCA platform with multilayer architecture for wire crossing. The designed 1:4 multiplexer requires 9 Majority gates, one inverter with the utilization of 90 cells, and area coverage is 0.13μm^2. The proposed 4:1 demultiplexer consists of 192 cells, 8 majority gates with 0.19μm^2 area coverage. The 2 bit counter uses a D flip-flop designed with 85 compartments, one two-input exclusive OR gate,

and it occupies a 0.09 μm^2 area. The pulse generator is designed with 3 majority gates, 27 cells with a 0.04 μm^2 area. The single router is designed with 25 majority gates with 734 cells and it occupies a 1.51 μm^2 space. Also, it utilized multilayer crossover for getting the correct output. The 4x4 Nano router utilizes 100 majority gates with 3693cells. Multilayer crossover is used for the complete design structure. From the analysis, the comparison and simulation results of the proposed circuit prove the functional efficiency of the course. The proposed design will play an essential role in low cost and low energy at nanoscale communication with low energy levels.

CHAPTER 8

CONCLUSION AND FUTURE ENHANCEMENT

This chapter details the summary and future enhancement of the proposed research.

8.1 CONCLUSION

QCA circuits are created in this study by making use of the QCA logic, which is discussed in detail below. Three-input Exclusive OR gate, one-bit Full adder, one-bit Full subtractor, pulse generator, D type flip-flop, synchronous counter, 4:1 Multiplexer, and one-fourth Demultiplexer are suggested, constructed, and simulated based on QCA technology.

According to past research in this field, all of the designs are innovative, modular, and optimum. It is the goal of this study to accomplish data transmission with reduced complexity design and low energy dissipation at the nanoscale level. Digital Nano communication with ultra-low energy dissipation is achieved by the use of the suggested QCA circuits.

The optimality of the recommended circuits is determined by comparing the area occupied, the number of cells and the latency to that of previous research in this field. It has been discovered that the suggested TIEO has fewer cells and less area when compared to existing designs. In our suggested plan, to get high performance with less count by the use three-input

XOR gate design with a single layer. The suggested adder and subtractor perform reliably well. Its clocking phase is realized fast. In proposed complete adder plan uses 44 cells to design1and 31cells in desgin2 with two clock phases and a 0.02 µm2 area approximately as shown in Fig 12. Similar way the proposed design of the full subtractor uses 43cells in design1 and 30 cells in design2 with two clock phases and a 0.02 µm2 area approximately. Also average power dissipation of full adder is 2.83e-003 eV with Error voltage 2.83e-004 eV and average power dissipation for full subtractor 2.41e-003 eV with Error voltage -2.45e-004 eV can be obtained with QCADesigner E tool. When compared to previous designs, the suggested circuit's one-bit full adder and full subtractor are constructed with fewer cells and less space.

In second phase, to designed and compared D-type flip-flop and counter by divide by 2 counter concept. Among all the structures, the proposed construction of the D flip-flop is achieved less and the proposed 2 bit counter achieved a 30% improvement in terms of cell count and latency respectively. In this the proposed D-type flip-flop has fewer cells, less latency, and less area.

Finally, when comparing the nano router, the proposed nano router has fewer cells and less surface area. The designed Nano router structure is realized in the QCA platform with multilayer architecture for wire crossing. The designed 1:4 multiplexer requires 9 Majority gates, one inverter with the utilization of 90 cells, and area coverage is 0.13µm2. The proposed 4:1 demultiplexer consists of 192 cells, 8 majority gates with 0.19µm2 area coverage. The 2 bit counter uses a D flip-flop designed with 85 compartments, one two-input exclusive OR gate, and it occupies a 0.09 µm2 area. The pulse generator is designed with 3 majority gates, 27 cells with a

0.04 μm2 area. The single router is designed with 25 majority gates with 734 cells and it occupies a 1.51 μm2 space. Also, it utilized multilayer crossover for getting the correct output. The 4x4 Nano router utilizes 100 majority gates with 3693cells. Multilayer crossover is used for the complete design structure. QCA designer and QCA designer E are two tools that may be used to simulate and analyze a QCA design and its results. From the analysis, the comparison and simulation results of the proposed circuit prove the functional efficiency of the course. The proposed design will play an essential role in low cost and low energy at nanoscale communication with low energy levels.

The donations prepared in the planned research are recorded below

- The optimized TIEO, Full adder, and Full subtractor in QCA technology is successfully designed and simulated.
- Optimized D type Flip-flop and counter circuits at a nanoscale level designed, implemented, and simulated successfully.
- Successfully modeled, designed, and simulated a novel QCA based nano router for high-speed data transmission which includes a feature for a high-speed crossbar scheduler.
- The proposed circuits are compared with the existing QCA circuits. The proposed designs have improved optimization about less numbers of cells used, the area occupied, and latency.

8.2 FUTURE ENCHANCEMENT

Using metal dot QCA implementation, it is possible to implement the circuits developed in this investigation. Although it is commonly known that metal dot QCA devices can only work at cryogenic temperatures, it is not

well understood why. Recent research, on the other hand, has shown that these circuits can operate at room temperature if the dimensions are just slightly expanded. QCA circuits based on molecular and magnetic QCA technology can also work at room temperature. Future research may be carried out to improve the suggested circuits for use in molecular and magnetic QCA implementation, among other things.

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1. **Kalpana, K** & Paulchamy, B 2021, 'A Novel design of Nano router with high speed crossbar scheduler for digital systems in QCA paradigm', Circuit World-Emerald Publishing. vol. 48, no. 44, pp. 464-468. https://doi.org /10.1108 /CW-10-2020-0280, **Impact Factor: 1.026.**